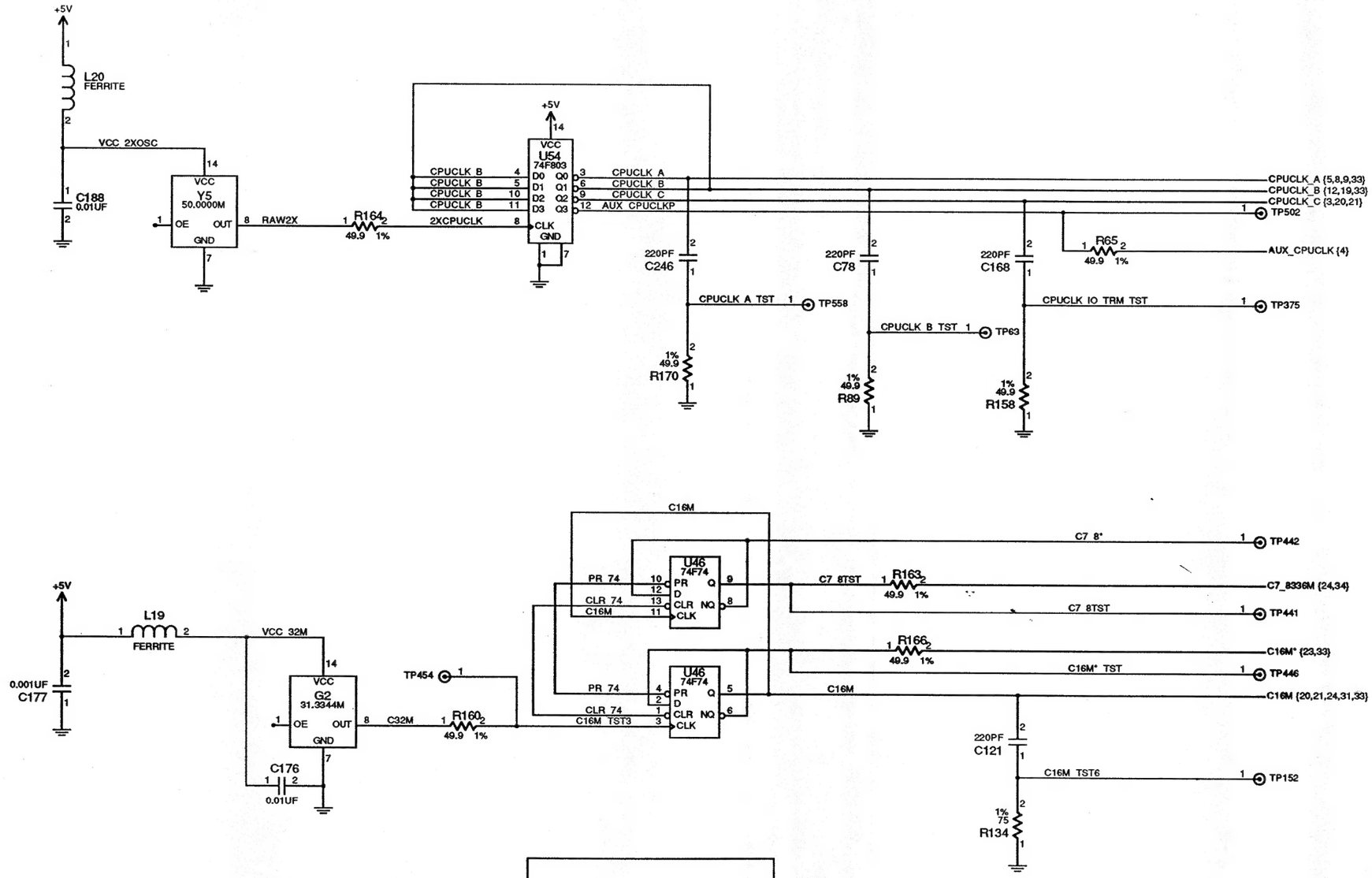

CPUCLK and IOCLK Oscillators

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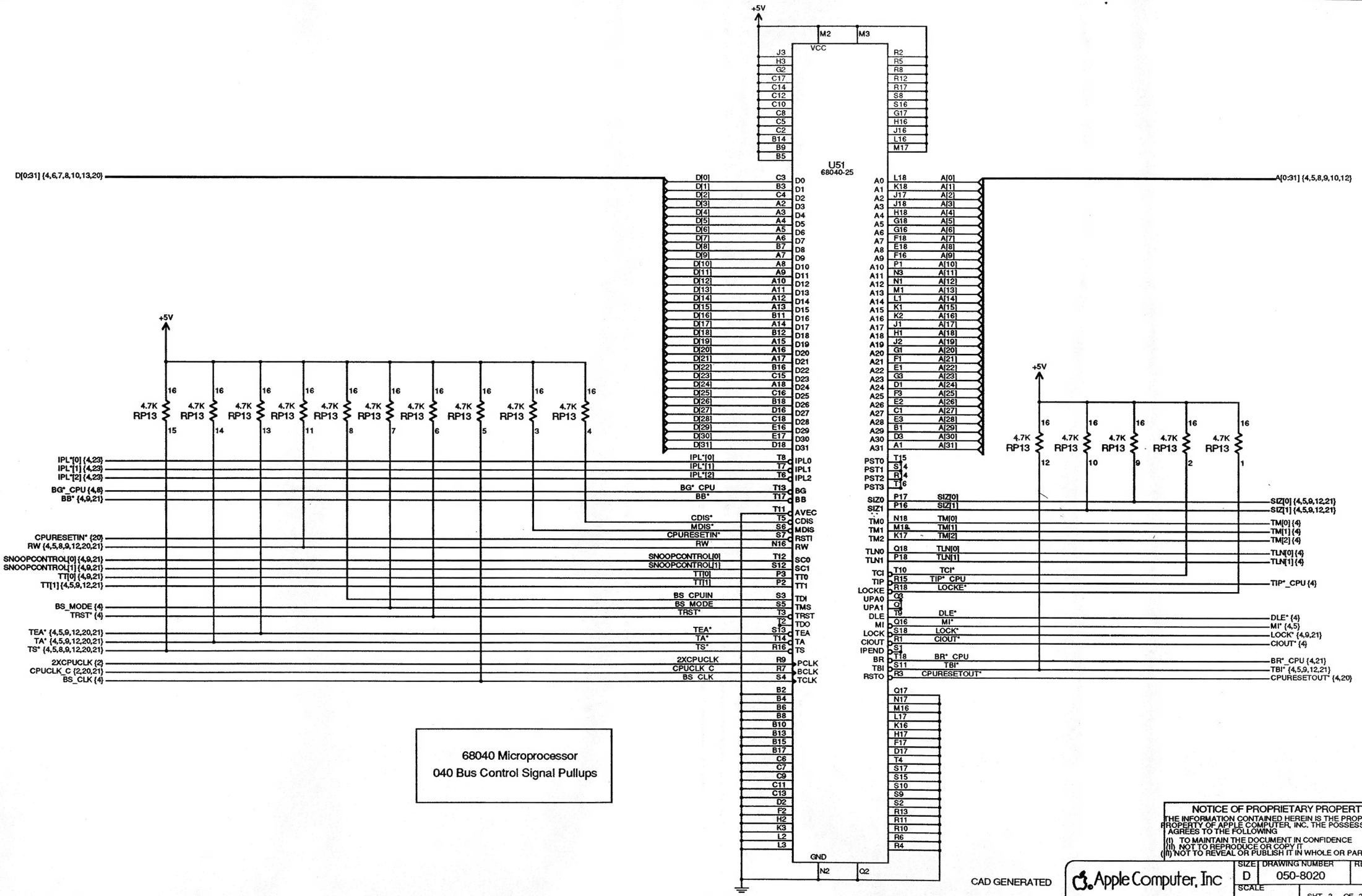
+5V
M2
M3
VCC
U51
68040-25
J3
H3
G2
C17
C14
C12
C10
C8
C5
C2
B14
B9
B5
R2
R5
R8
R12
R17
S8
S16
G17
H16
J16
L16
M17
D[0:31] {4,6,7,8,10,13,20}
D[0] C3 D0
D[1] B3 D1
D[2] C4 D2
D[3] A2 D3
D[4] A3 D4
D[5] A4 D5
D[6] A5 D6
D[7] A6 D7
D[8] B7 D8
D[9] A7 D9
D[10] A8 D10
D[11] A9 D11
D[12] A10 D12
D[13] A11 D13
D[14] A12 D14
D[15] A13 D15
D[16] B11 D16
D[17] A14 D17
D[18] B12 D18
D[19] A15 D19
D[20] A16 D20
D[21] A17 D21
D[22] B16 D22
D[23] C15 D23
D[24] A18 D24
D[25] C16 D25
D[26] B18 D26
D[27] D16 D27
D[28] C18 D28
D[29] E16 D29
D[30] E17 D30
D[31] D18 D31
A0 L18 A[0]
A1 K18 A[1]
A2 J17 A[2]
A3 J18 A[3]
A4 H18 A[4]
A5 G18 A[5]
A6 G16 A[6]
A7 F18 A[7]
A8 E18 A[8]
A9 F16 A[9]
A10 P1 A[10]
A11 N3 A[11]
A12 N1 A[12]
A13 M1 A[13]
A14 L1 A[14]
A15 K1 A[15]
A16 K2 A[16]
A17 J1 A[17]
A18 H1 A[18]
A19 J2 A[19]
A20 G1 A[20]
A21 F1 A[21]
A22 E1 A[22]
A23 G3 A[23]
A24 D1 A[24]
A25 F3 A[25]
A26 E2 A[26]
A27 C1 A[27]
A28 E3 A[28]
A29 B1 A[29]
A30 D3 A[30]
A31 A1 A[31]
A[0:31] {4,5,8,9,10,12}
PST0 T15
PST1 S14
PST2 R14
PST3 T16
SIZ0 P17 SIZ[0]
SIZ1 P16 SIZ[1]
SIZ[0] {4,5,9,12,21}
SIZ[1] {4,5,9,12,21}
TM0 N18 TM[0]
TM1 M18 TM[1]
TM2 K17 TM[2]
TM[0] {4}
TM[1] {4}
TM[2] {4}
TLN0 Q18 TLN[0]
TLN1 P18 TLN[1]
TLN[0] {4}
TLN[1] {4}
TCI T10 TCI*
TIP R15 TIP* CPU
LOCKE R18 LOCKE*
TIP*_CPU {4}
UPA0 Q3
UPA1 Q1
DLE T9 DLE*
MI Q16 MI*
LOCK S18 LOCK*
CIOUT R1 CIOUT*
IPEND S1
BR T18 BR* CPU
TBI S11 TBI*
RSTO R3 CPURESETOUT*
DLE* {4}
MI* {4,5}
LOCK* {4,9,21}
CIOUT* {4}
BR*_CPU {4,21}
TBI* {4,5,9,12,21}
CPURESETOUT* {4,20}
+5V
4.7K RP13 16 15
4.7K RP13 16 14
4.7K RP13 16 13
4.7K RP13 16 11
4.7K RP13 16 8
4.7K RP13 16 7
4.7K RP13 16 6
4.7K RP13 16 5
4.7K RP13 16 3
4.7K RP13 16 4
IPL*[0] {4,23}
IPL*[1] {4,23}
IPL*[2] {4,23}
BG*_CPU {4,8}
BB* {4,9,21}
CPURESETIN* {20}
RW {4,5,8,9,12,20,21}
SNOOPCONTROL[0] {4,9,21}
SNOOPCONTROL[1] {4,9,21}
TT[0] {4,9,21}
TT[1] {4,5,9,12,21}
BS_MODE {4}
TRST* {4}
TEA* {4,5,9,12,20,21}
TA* {4,5,9,12,20,21}
TS* {4,5,8,9,12,20,21}
2XCPUCLK {2}
CPUCLK_C {2,20,21}
BS_CLK {4}
IPL*[0] T8 IPL0
IPL*[1] T7 IPL1
IPL*[2] T6 IPL2
BG*_CPU T13 BG
BB* T17 BB
AVEC T11
CDIS* T5 CDIS
MDIS* S6 MDIS
CPURESETIN* S7 RSTI
RW N16 RW
SNOOPCONTROL[0] T12 SC0
SNOOPCONTROL[1] S12 SC1
TT[0] P3 TT0
TT[1] P2 TT1
BS_CPUIN S3 TDI
BS_MODE S5 TMS
TRST* T3 TRST
T2 TDO
TEA* S13 TEA
TA* T14 TA
TS* R16 TS
2XCPUCLK R9 PCLK
CPUCLK_C R7 BCLK
BS_CLK S4 TCLK
B2
B4
B6
B8
B10
B13
B15
B17
C6
C7
C9
C11
C13
D2
F2
H2
K3
L2
L3
Q17
N17
M16
L17
K16
H17
F17
D17
T4
S17
S15
S10
S9
S2
R13
R11
R10
R6
R4
GND
N2
Q2
+5V
4.7K RP13 16 12
4.7K RP13 16 10
4.7K RP13 16 9
4.7K RP13 16 2
4.7K RP13 16 1
68040 Microprocessor
040 Bus Control Signal Pullups
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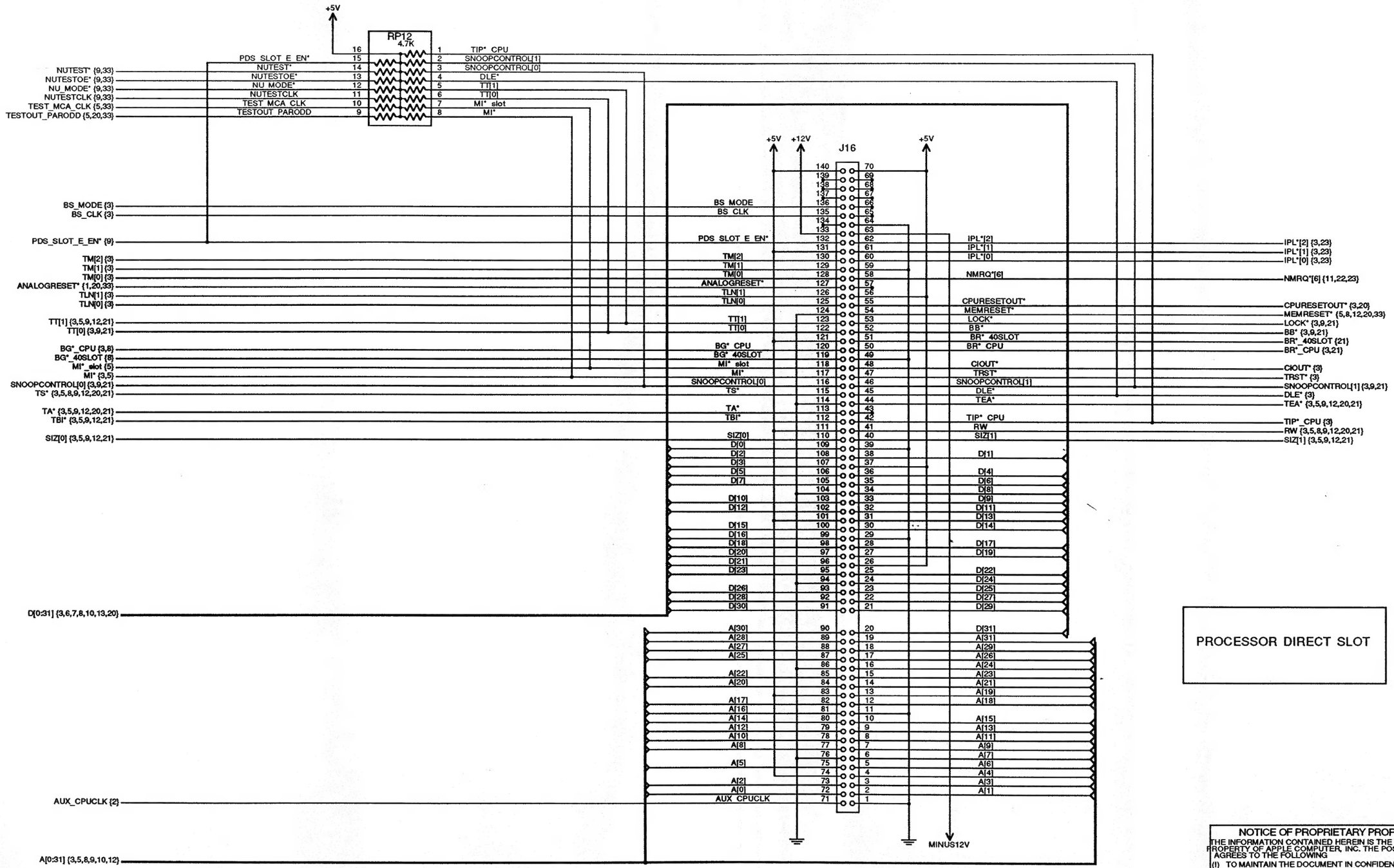

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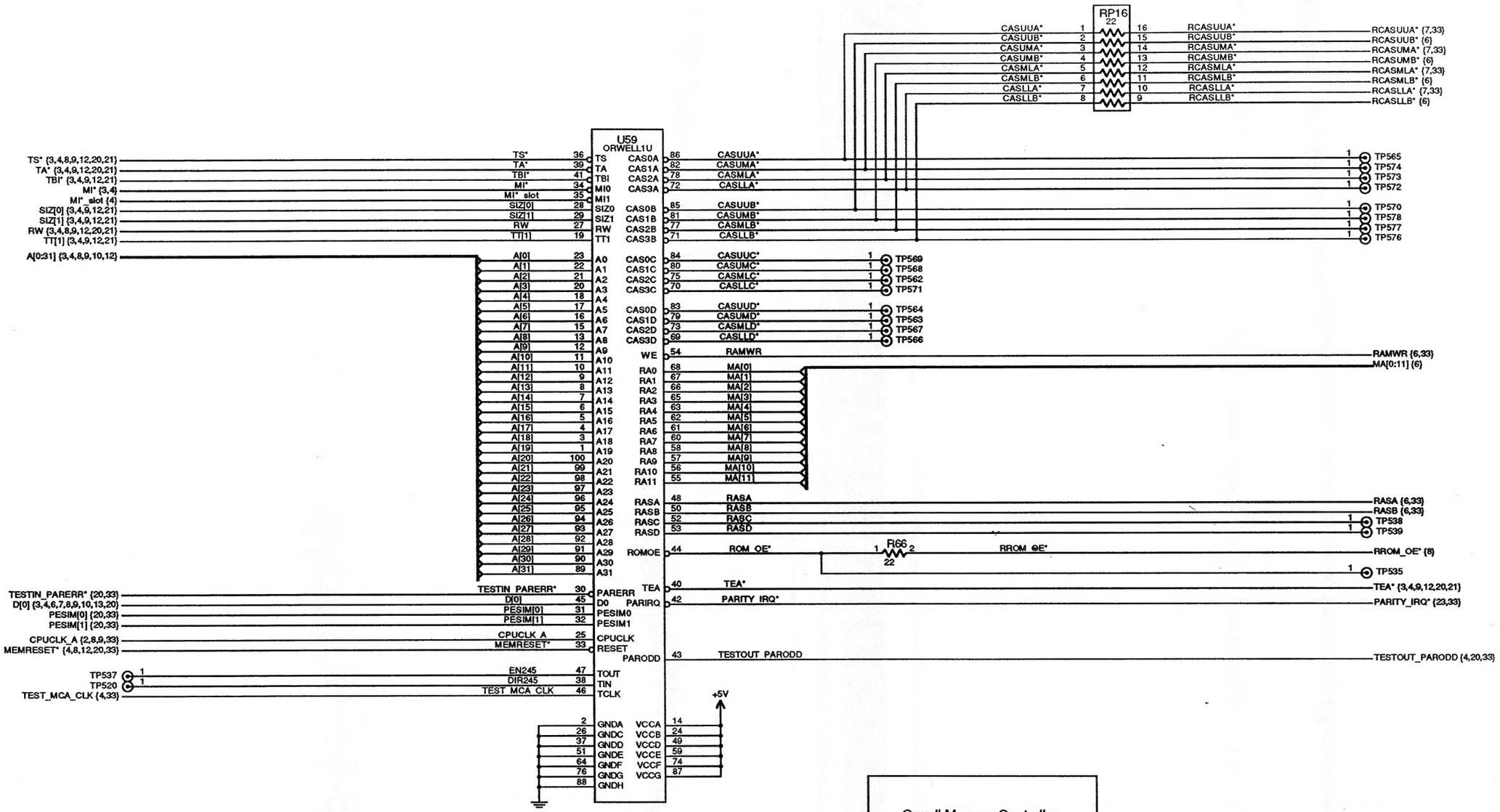

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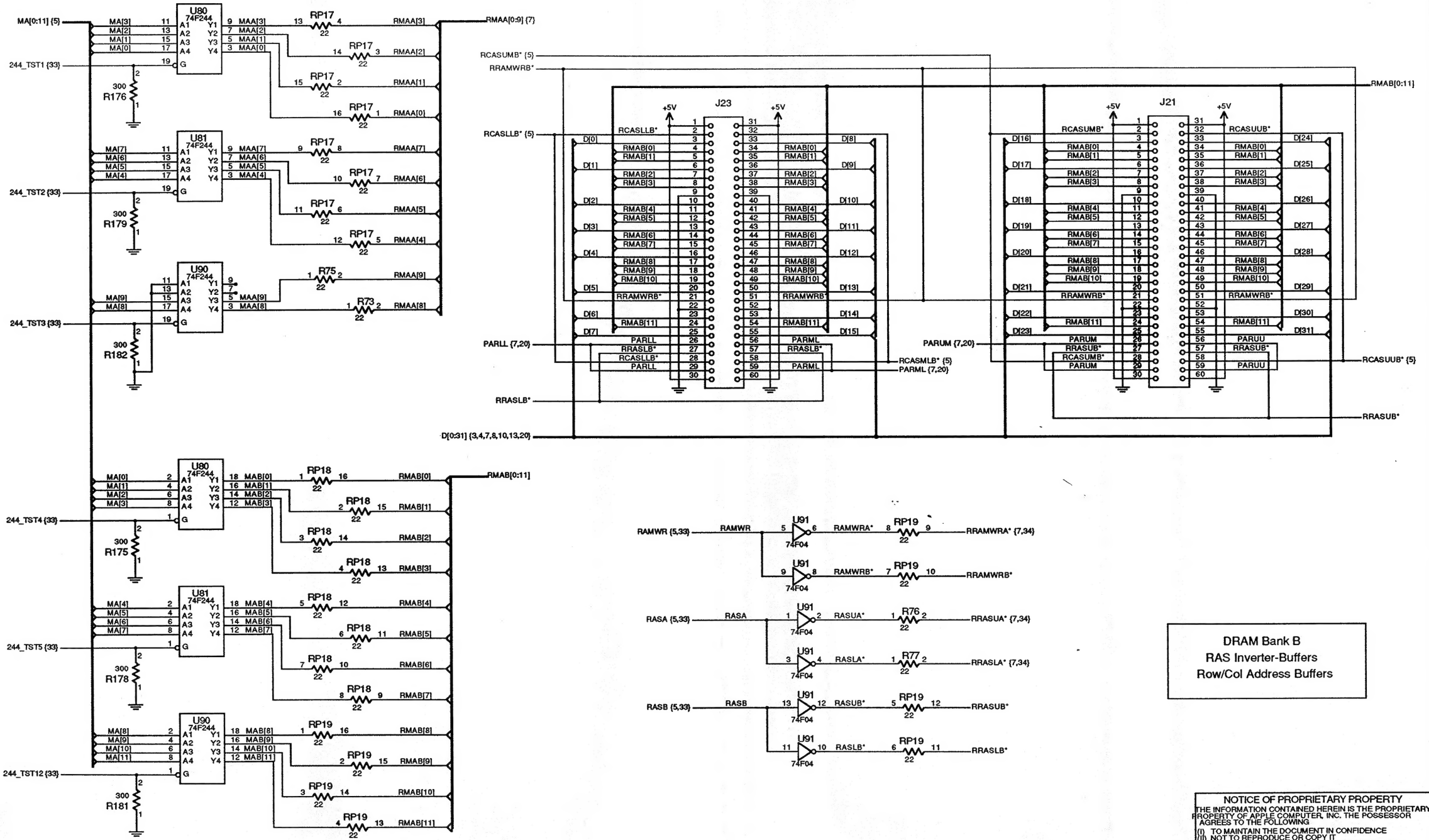

DRAM Bank B
RAS Inverter-Buffers
Row/Col Address Buffers

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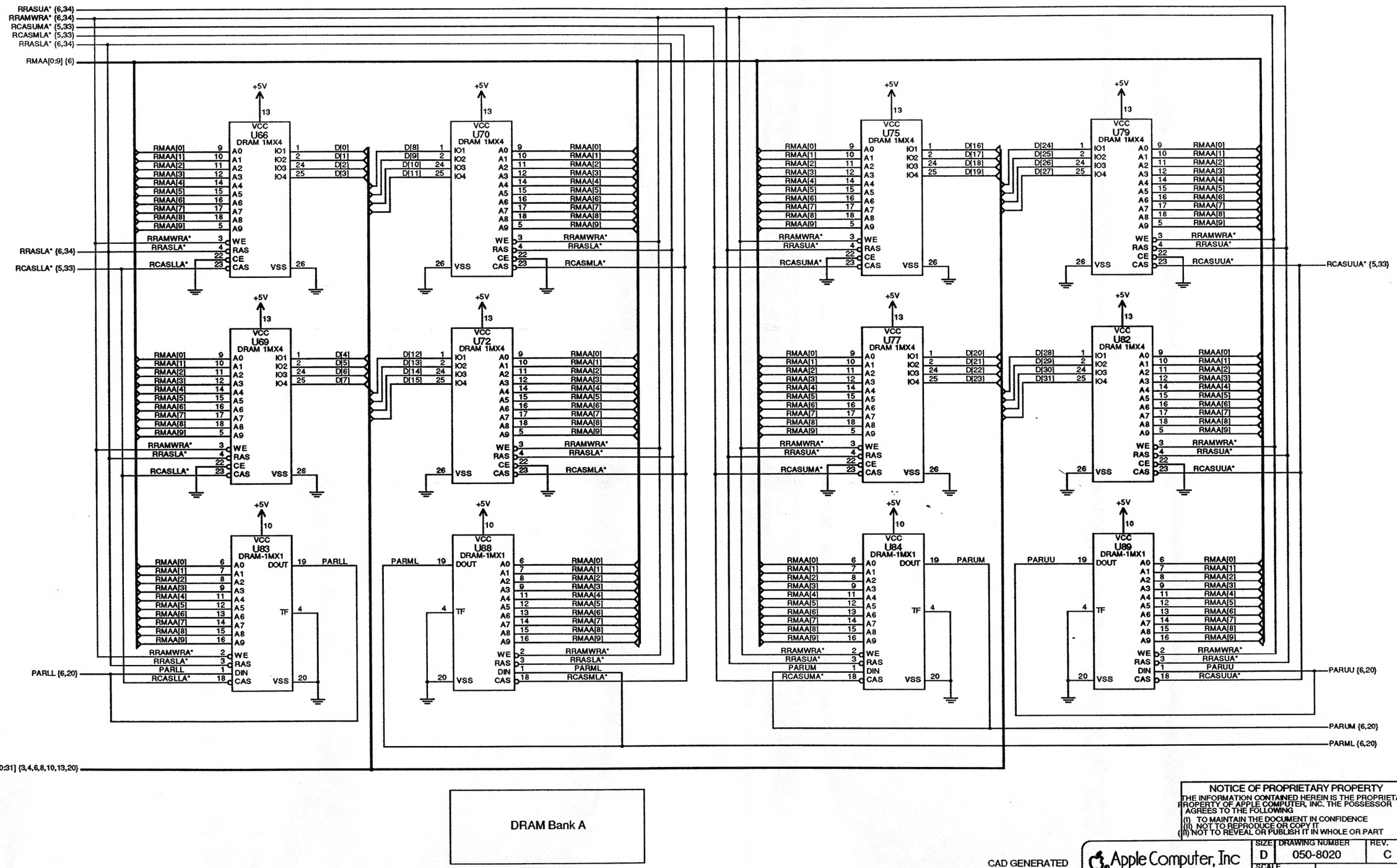

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RROM_OE* {5}

D[0:31] {3,4,6,7,10,13,20}

ROM SOP CE*

ROM SIMM must have pin 11 connected to +5v
and the CE* on the ROM SIMM must be tied to GND
This eliminates need for ROM source select jumper

ROM LOW

U74
ROM 256KX16
VDD 21
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15/A-1
CE/CE
OE
BYTE
GND1 GND2 11 30

A[2] 9 A[3] 8 A[4] 7 A[5] 6 A[6] 5 A[7] 4 A[8] 3 A[9] 2 A[10] 40 A[11] 39 A[12] 38 A[13] 37 A[14] 36 A[15] 35 A[16] 34 A[17] 33 A[18] 32 A[19] 1
ROM_SOP_CE* 10
RROM_OE* 12
31

D[0] 13 D[1] 15 D[2] 17 D[3] 19 D[4] 22 D[5] 24 D[6] 26 D[7] 28 D[8] 14 D[9] 16 D[10] 18 D[11] 20 D[12] 23 D[13] 25 D[14] 27 D[15] 29

ROM HIGH

U68
ROM 256KX16
VDD 21
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15/A-1
CE/CE
OE
BYTE
GND1 GND2 11 30

A[2] 9 A[3] 8 A[4] 7 A[5] 6 A[6] 5 A[7] 4 A[8] 3 A[9] 2 A[10] 40 A[11] 39 A[12] 38 A[13] 37 A[14] 36 A[15] 35 A[16] 34 A[17] 33 A[18] 32 A[19] 1
ROM_SOP_CE* 10
RROM_OE* 12
31

D[16] 13 D[17] 15 D[18] 17 D[19] 19 D[20] 22 D[21] 24 D[22] 26 D[23] 28 D[24] 14 D[25] 16 D[26] 18 D[27] 20 D[28] 23 D[29] 25 D[30] 27 D[31] 29

300 R177 2 1

+5V +12V +5V

J18

	1	2	
FLASH_WE*	3	4	A[2]
A[3]	5	6	A[4]
A[5]	7	8	A[6]
A[7]	9	10	
ROM_SOP_CE*	11	12	RROM_OE*
	13	14	D[0]
D[1]	15	16	D[2]
D[3]	17	18	D[4]
D[5]	19	20	D[6]
D[7]	21	22	D[8]
D[9]	23	24	D[10]
D[11]	25	26	D[12]
D[13]	27	28	D[14]
D[15]	29	30	
A[8]	31	32	A[9]
A[10]	33	34	A[11]
A[12]	35	36	A[13]
A[14]	37	38	A[15]
A[16]	39	40	A[17]
A[18]	41	42	A[19]
A[20]	43	44	A[21]
A[22]	45	46	
D[16]	47	48	D[17]
D[18]	49	50	D[19]
D[20]	51	52	D[21]
D[22]	53	54	D[23]
D[24]	55	56	D[25]
D[26]	57	58	D[27]
D[28]	59	60	D[29]
D[30]	61	62	D[31]
	63	64	

A[0:31] {3,4,5,9,10,12}

U64
PAL20R8B
I0 I1 I2 I3 I4 I5 I6 I7 I8 I9 I10 I11
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
OE
CLK

A[31] 3 A[30] 4 A[29] 5 A[28] 6 A[22] 7 MEMRESET* 9 RW 10 TS* 11 PRE_BG*_CPU 12 PRE_BG*_40SLOT 13 BGACK* 17 27 FA_PAL_EN* 16 CPUCLK_A 2

26 25 BG*_CPU 24 BG*_40SLOT 23 FA_ST0* 21 FA_ST1* 20 FLASH_WE* 19 BGACK_2* 18 BGACK_1*

BG*_CPU {3,4}
BG*_40SLOT {4}
1 TP702
1 TP703
1 TP704
1 TP705

MEMRESET* {4,5,12,20,33}
RW {3,4,5,9,12,20,21}
TS* {3,4,5,9,12,20,21}
PRE_BG*_CPU {21,33}
PRE_BG*_40SLOT {21,33}
BGACK* {21,22,31,33}

TP706 1
CPUCLK_A {2,5,9,33}

300 R33 2 1

ROM
ROM SIMM
Flash ROM/Bus Arb Control PAL

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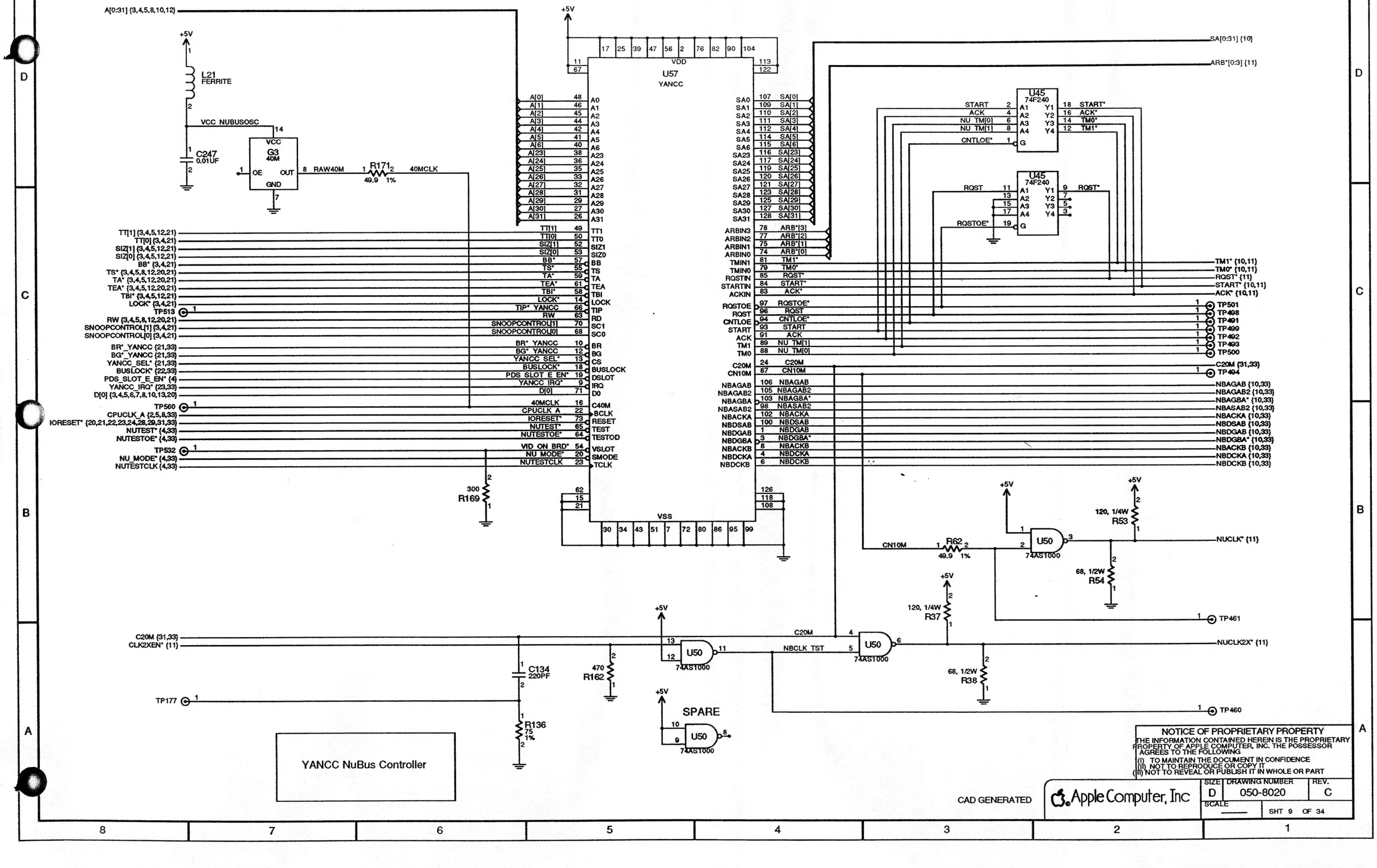
A[0:31] {3,4,5,8,10,12}
+5V
L21
FERRITE
VCC_NUBUSOSC
C247
0.01UF
G3
40M
OE
OUT
GND
RAW40M
R171
49.9 1%
40MCLK
U57
YANCC
VDD
VSS
SA[0:31] {10}
ARB*[0:3] {11}
U45
74F240
START
ACK
NU_TM[0]
NU_TM[1]
CNTLOE*
RQST
RQSTOE*
TM1* {10,11}
TM0* {10,11}
RQST* {11}
START* {10,11}
ACK* {10,11}
C20M {31,33}
NBAGAB {10,33}
NBAGAB2 {10,33}
NBAGBA* {10,33}
NBASAB2 {10,33}
NBACKA {10,33}
NBDSAB {10,33}
NBDGAB {10,33}
NBDGBA* {10,33}
NBACKB {10,33}
NBDCKA {10,33}
NBDCKB {10,33}
TP501
TP498
TP491
TP499
TP492
TP493
TP500
TP494
TT[1] {3,4,5,12,21}
TT[0] {3,4,21}
SIZ[1] {3,4,5,12,21}
SIZ[0] {3,4,5,12,21}
BB* {3,4,21}
TS* {3,4,5,8,12,20,21}
TA* {3,4,5,12,20,21}
TEA* {3,4,5,12,20,21}
TBI* {3,4,5,12,21}
LOCK* {3,4,21}
TP513
RW {3,4,5,8,12,20,21}
SNOOPCONTROL[1] {3,4,21}
SNOOPCONTROL[0] {3,4,21}
BR*_YANCC {21,33}
BG*_YANCC {21,33}
YANCC_SEL* {21,33}
BUSLOCK* {22,33}
PDS_SLOT_E_EN* {4}
YANCC_IRQ* {23,33}
D[0] {3,4,5,6,7,8,10,13,20}
TP560
CPUCLK_A {2,5,8,33}
IORESET* {20,21,22,23,24,28,29,31,33}
NUTEST* {4,33}
NUTESTOE* {4,33}
TP532
NU_MODE* {4,33}
NUTESTCLK {4,33}
300
R169
TP177
C20M {31,33}
CLK2XEN* {11}
C134
220PF
470
R162
R136
75
1%
SPARE
74AS1000
NBCLK_TST
NUCLK* {11}
NUCLK2X* {11}
R62
R53
R54
R37
R38
120, 1/4W
68, 1/2W
49.9 1%
TP461
TP460
YANCC NuBus Controller
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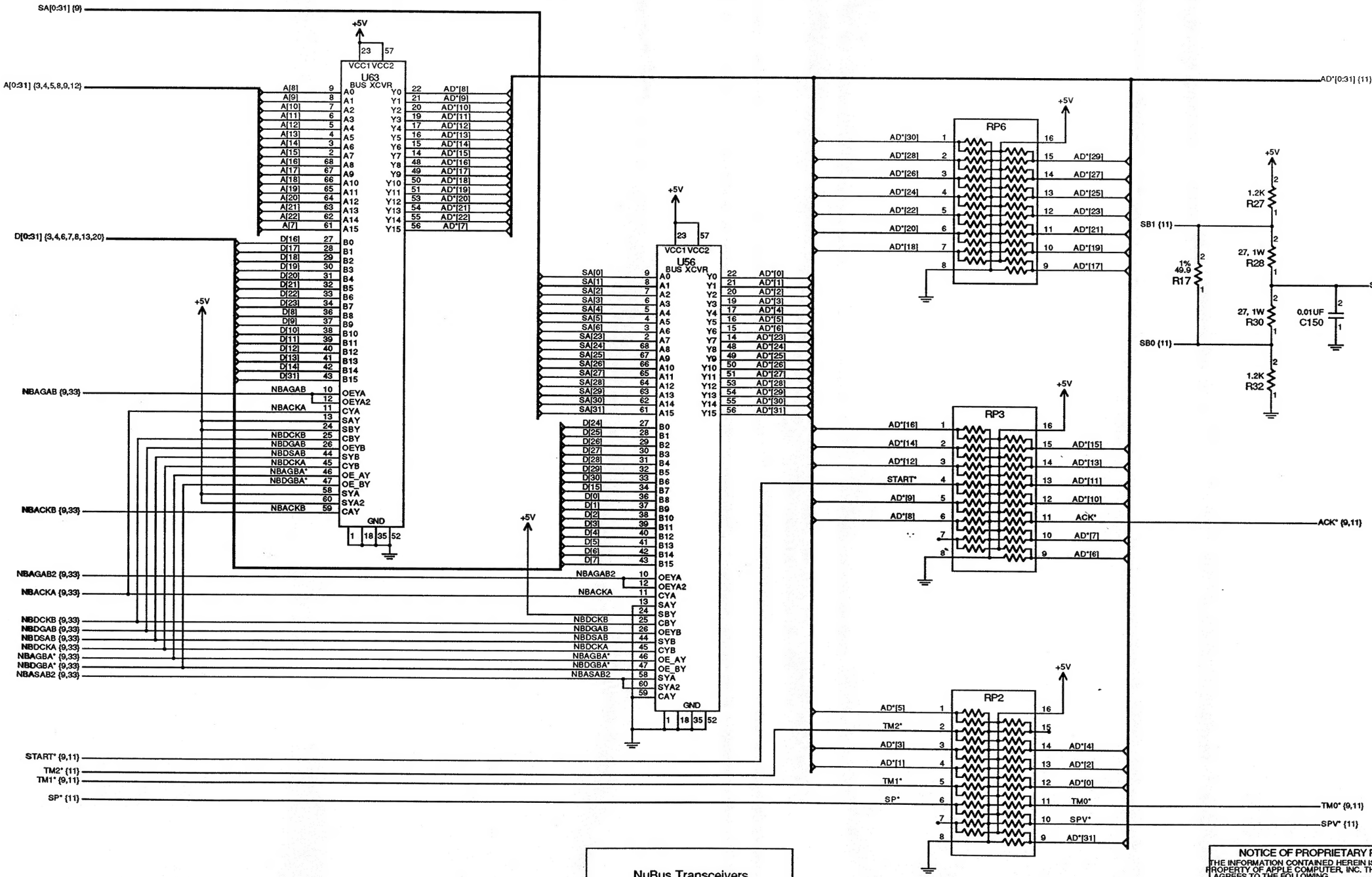

NuBus Transceivers
NuBus Termination RPAKs

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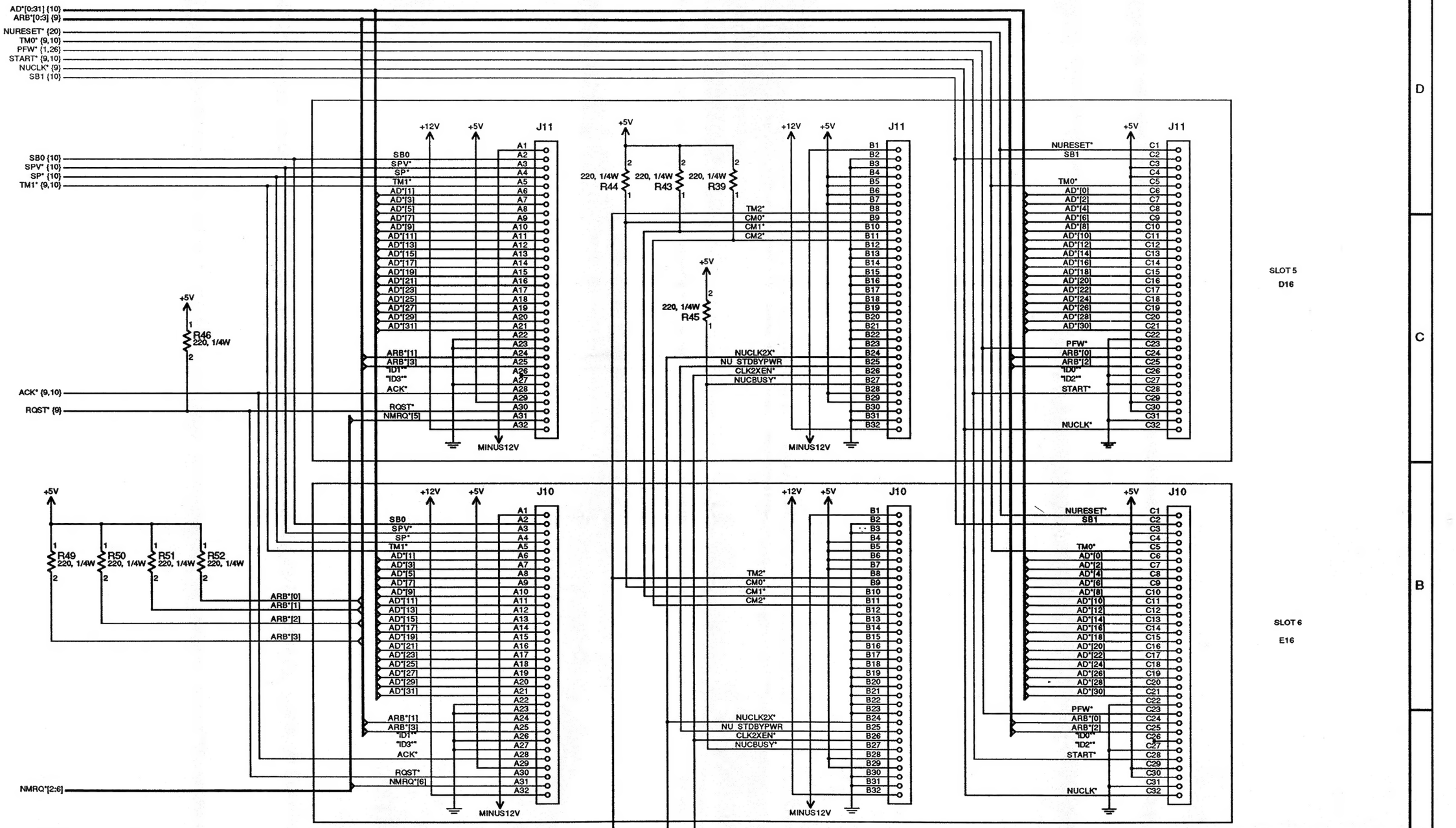
AD*[0:31] {10}
ARB*[0:3] {9}
NURESET* {20}
TM0* {9,10}
PFW* {1,26}
START* {9,10}
NUCLK* {9}
SB1 {10}
SB0 {10}
SPV* {10}
SP* {10}
TM1* {9,10}
ACK* {9,10}
RQST* {9}
TM2* {10}
NUCLK2X* {9}
CLK2XEN* {9}
NMRQ*[2:6]
R46 220, 1/4W
R44 220, 1/4W
R43 220, 1/4W
R39 220, 1/4W
R45 220, 1/4W
R49 220, 1/4W
R50 220, 1/4W
R51 220, 1/4W
R52 220, 1/4W
+5V
+12V
MINUS12V
J11
J10
SLOT 5
D16
SLOT 6
E16
NuBus Slots D & E
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SHT 11 OF 34
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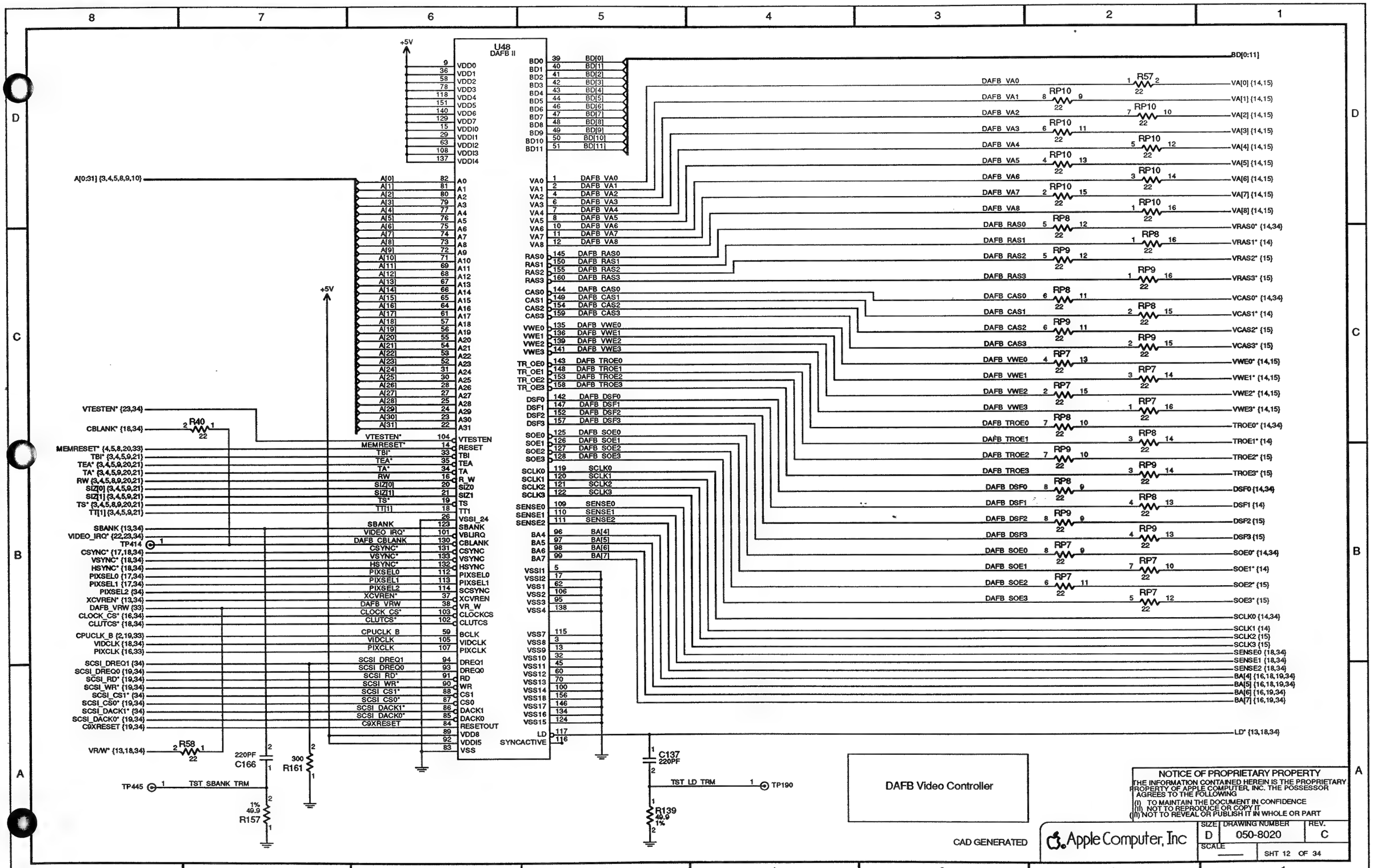
U48
DAFB II
+5V
VDD0
VDD1
VDD2
VDD3
VDD4
VDD5
VDD6
VDD7
VDDI0
VDDI1
VDDI2
VDDI3
VDDI4
A[0:31] {3,4,5,8,9,10}
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
A21
A22
A23
A24
A25
A26
A27
A28
A29
A30
A31
VTESTEN* {23,34}
CBLANK* {18,34}
R40
22
MEMRESET* {4,5,8,20,33}
TBI* {3,4,5,9,21}
TEA* {3,4,5,9,20,21}
TA* {3,4,5,9,20,21}
RW {3,4,5,8,9,20,21}
SIZ[0] {3,4,5,9,21}
SIZ[1] {3,4,5,9,21}
TS* {3,4,5,8,9,20,21}
TT[1] {3,4,5,9,21}
SBANK {13,34}
VIDEO_IRQ* {22,23,34}
TP414
CSYNC* {17,18,34}
VSYNC* {18,34}
HSYNC* {18,34}
PIXSEL0 {17,34}
PIXSEL1 {17,34}
PIXSEL2 {34}
XCVREN* {13,34}
DAFB_VRW {33}
CLOCK_CS* {16,34}
CLUTCS* {18,34}
CPUCLK_B {2,19,33}
VIDCLK {18,34}
PIXCLK {16,33}
SCSI_DREQ1 {34}
SCSI_DREQ0 {19,34}
SCSI_RD* {19,34}
SCSI_WR* {19,34}
SCSI_CS1* {34}
SCSI_CS0* {19,34}
SCSI_DACK1* {34}
SCSI_DACK0* {19,34}
C9XRESET {19,34}
VR/W* {13,18,34}
R58
22
220PF
C166
TP445
TST_SBANK_TRM
1%
49.9
R157
300
R161
VTESTEN*
MEMRESET*
TBI*
TEA*
TA*
RW
SIZ0
SIZ1
TS*
TT1
VSSI_24
SBANK
VIDEO_IRQ*
DAFB_CBLANK
CSYNC*
VSYNC*
HSYNC*
PIXSEL0
PIXSEL1
SCSYNC
XCVREN*
DAFB_VRW
CLOCK_CS*
CLUTCS*
BCLK
VIDCLK
PIXCLK
DREQ1
DREQ0
SCSI_RD*
SCSI_WR*
SCSI_CS1*
SCSI_CS0*
SCSI_DACK1*
SCSI_DACK0*
C9XRESET
VDD8
VDDI5
VSS
BD[0:11]
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BD8
BD9
BD10
BD11
VA0
VA1
VA2
VA3
VA4
VA5
VA6
VA7
VA8
RAS0
RAS1
RAS2
RAS3
CAS0
CAS1
CAS2
CAS3
VWE0
VWE1
VWE2
VWE3
TR_OE0
TR_OE1
TR_OE2
TR_OE3
DSF0
DSF1
DSF2
DSF3
SOE0
SOE1
SOE2
SOE3
SCLK0
SCLK1
SCLK2
SCLK3
SENSE0
SENSE1
SENSE2
BA4
BA5
BA6
BA7
VSSI1
VSSI2
VSS1
VSS2
VSS3
VSS4
VSS7
VSS8
VSS9
VSS10
VSS11
VSS12
VSS13
VSS14
VSS15
VSS16
VSS17
VSS18
LD
SYNCACTIVE
C137
220PF
TST_LD_TRM
TP190
R139
49.9
1%
DAFB_VA0
DAFB_VA1
DAFB_VA2
DAFB_VA3
DAFB_VA4
DAFB_VA5
DAFB_VA6
DAFB_VA7
DAFB_VA8
DAFB_RAS0
DAFB_RAS1
DAFB_RAS2
DAFB_RAS3
DAFB_CAS0
DAFB_CAS1
DAFB_CAS2
DAFB_CAS3
DAFB_VWE0
DAFB_VWE1
DAFB_VWE2
DAFB_VWE3
DAFB_TROE0
DAFB_TROE1
DAFB_TROE2
DAFB_TROE3
DAFB_DSF0
DAFB_DSF1
DAFB_DSF2
DAFB_DSF3
DAFB_SOE0
DAFB_SOE1
DAFB_SOE2
DAFB_SOE3
R57
RP10
RP8
RP9
RP7
VA[0] {14,15}
VA[1] {14,15}
VA[2] {14,15}
VA[3] {14,15}
VA[4] {14,15}
VA[5] {14,15}
VA[6] {14,15}
VA[7] {14,15}
VA[8] {14,15}
VRAS0* {14,34}
VRAS1* {14}
VRAS2* {15}
VRAS3* {15}
VCAS0* {14,34}
VCAS1* {14}
VCAS2* {15}
VCAS3* {15}
VWE0* {14,15}
VWE1* {14,15}
VWE2* {14,15}
VWE3* {14,15}
TROE0* {14,34}
TROE1* {14}
TROE2* {15}
TROE3* {15}
DSF0 {14,34}
DSF1 {14}
DSF2 {15}
DSF3 {15}
SOE0* {14,34}
SOE1* {14}
SOE2* {15}
SOE3* {15}
SCLK0 {14,34}
SCLK1 {14}
SCLK2 {15}
SCLK3 {15}
SENSE0 {18,34}
SENSE1 {18,34}
SENSE2 {18,34}
BA[4] {16,18,19,34}
BA[5] {16,18,19,34}
BA[6] {16,19,34}
BA[7] {16,19,34}
LD* {13,18,34}
DAFB Video Controller
CAD GENERATED
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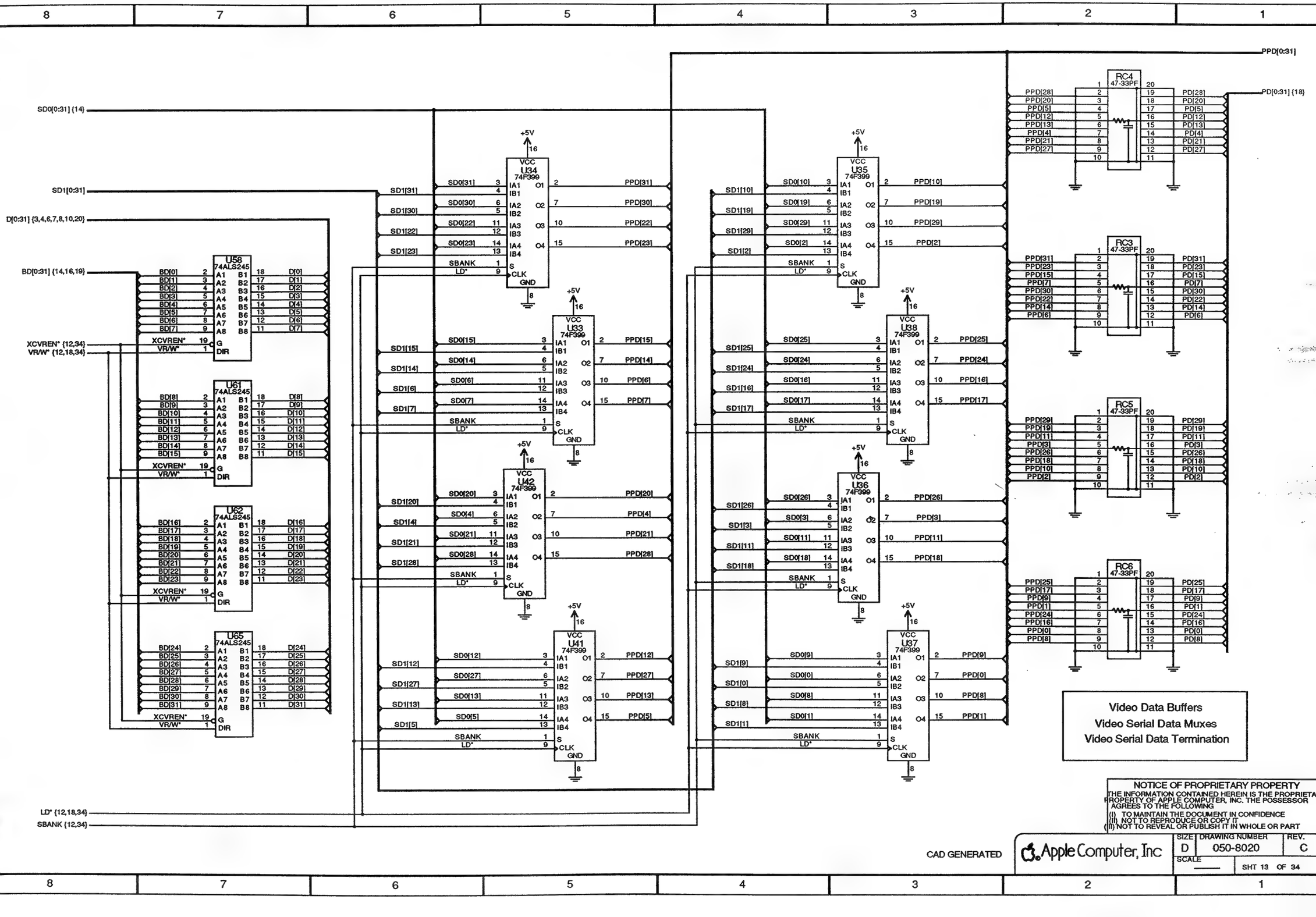
REV. C
SCALE
SHT 12 OF 34


SD0[0:31] {14}
SD1[0:31]
D[0:31] {3,4,6,7,8,10,20}
BD[0:31] {14,16,19}
XCVREN* {12,34}
VR/W* {12,18,34}
LD* {12,18,34}
SBANK {12,34}
PPD[0:31]
PD[0:31] {18}
U58 74ALS245
U61 74ALS245
U62 74ALS245
U65 74ALS245
U34 74F399
U33 74F399
U42 74F399
U41 74F399
U35 74F399
U38 74F399
U36 74F399
U37 74F399
RC4 47-33PF
RC3 47-33PF
RC5 47-33PF
RC6 47-33PF
Video Data Buffers
Video Serial Data Muxes
Video Serial Data Termination
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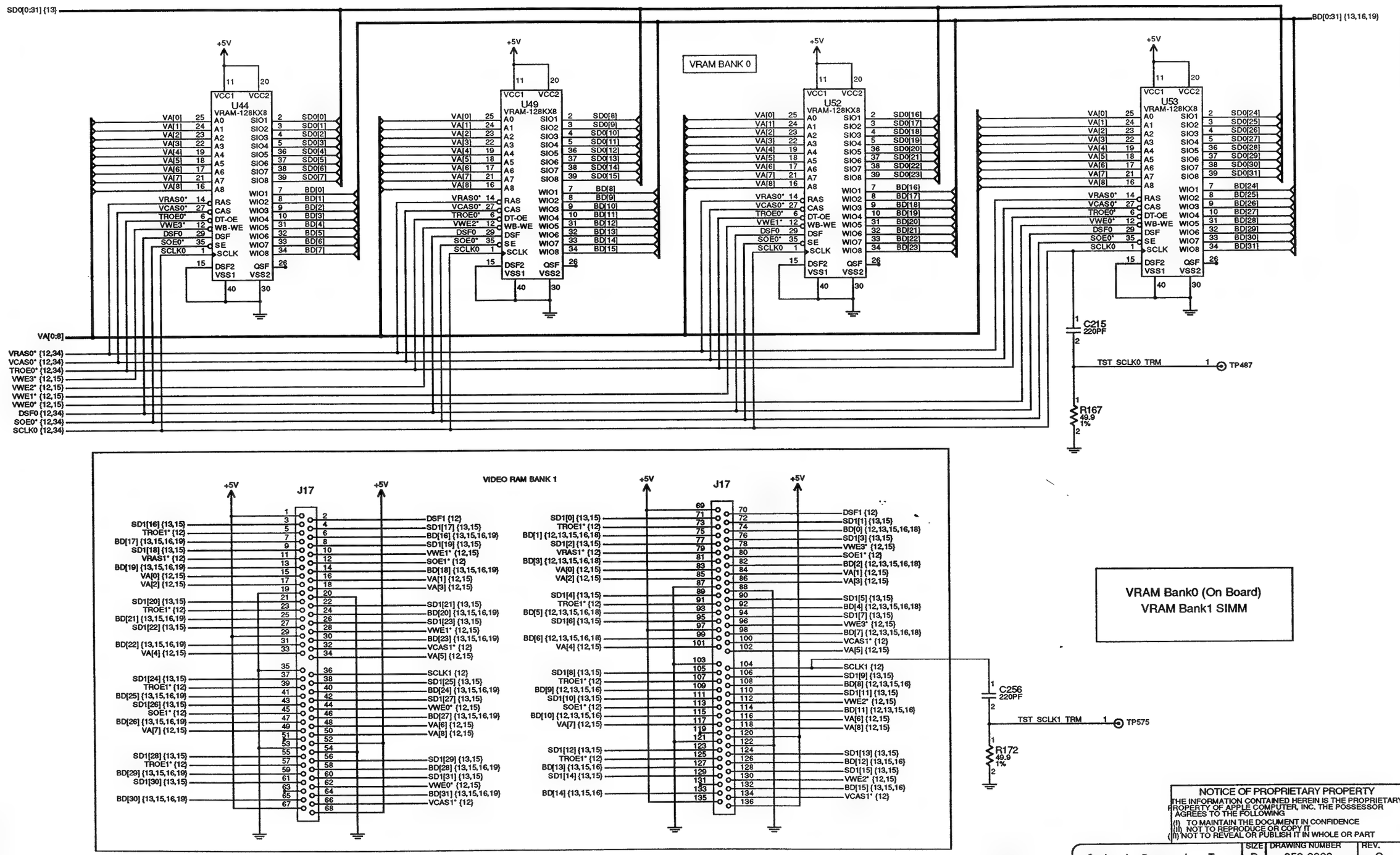

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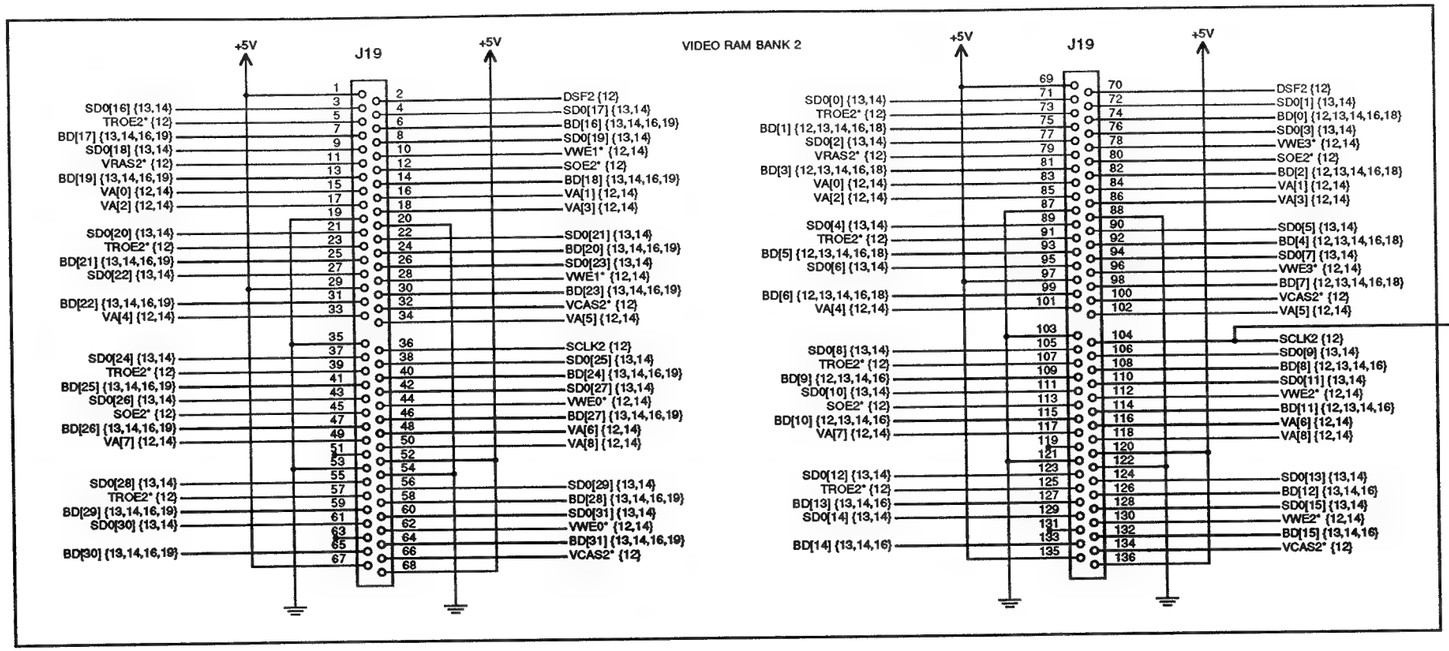

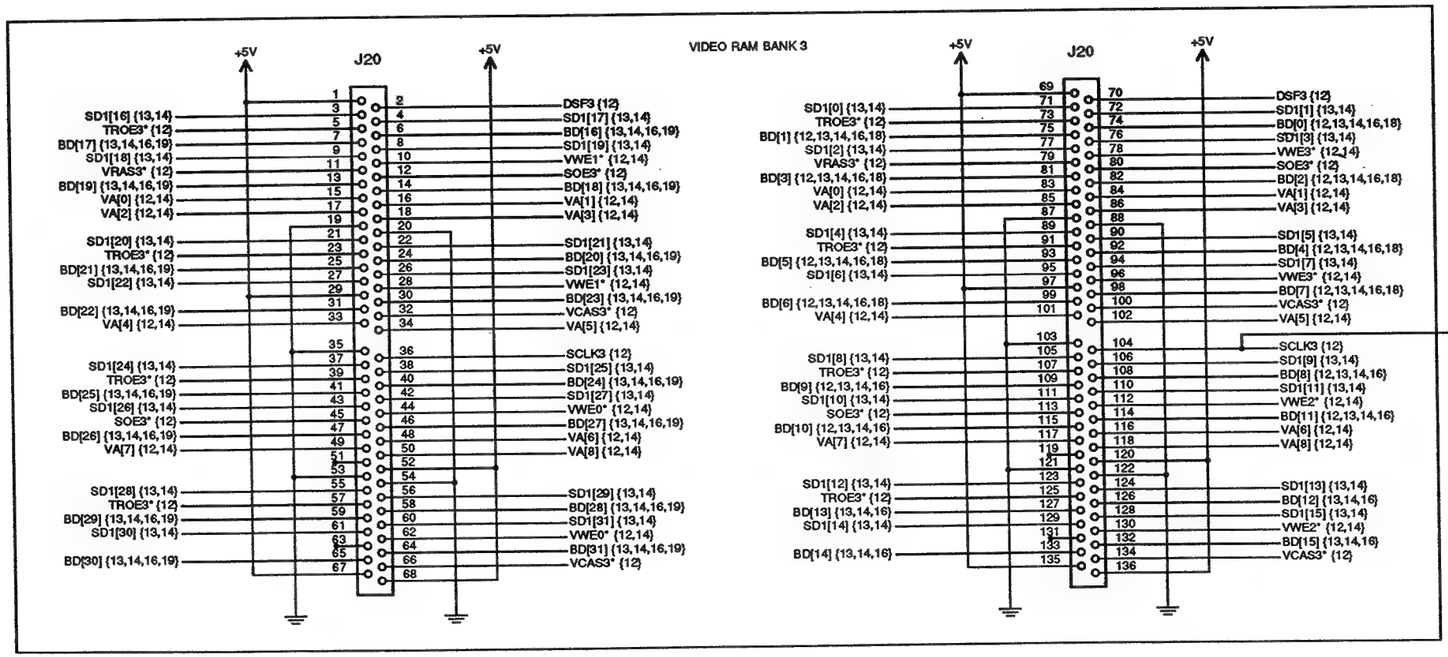

VRAM Banks 2 and 3 (SIMMS)

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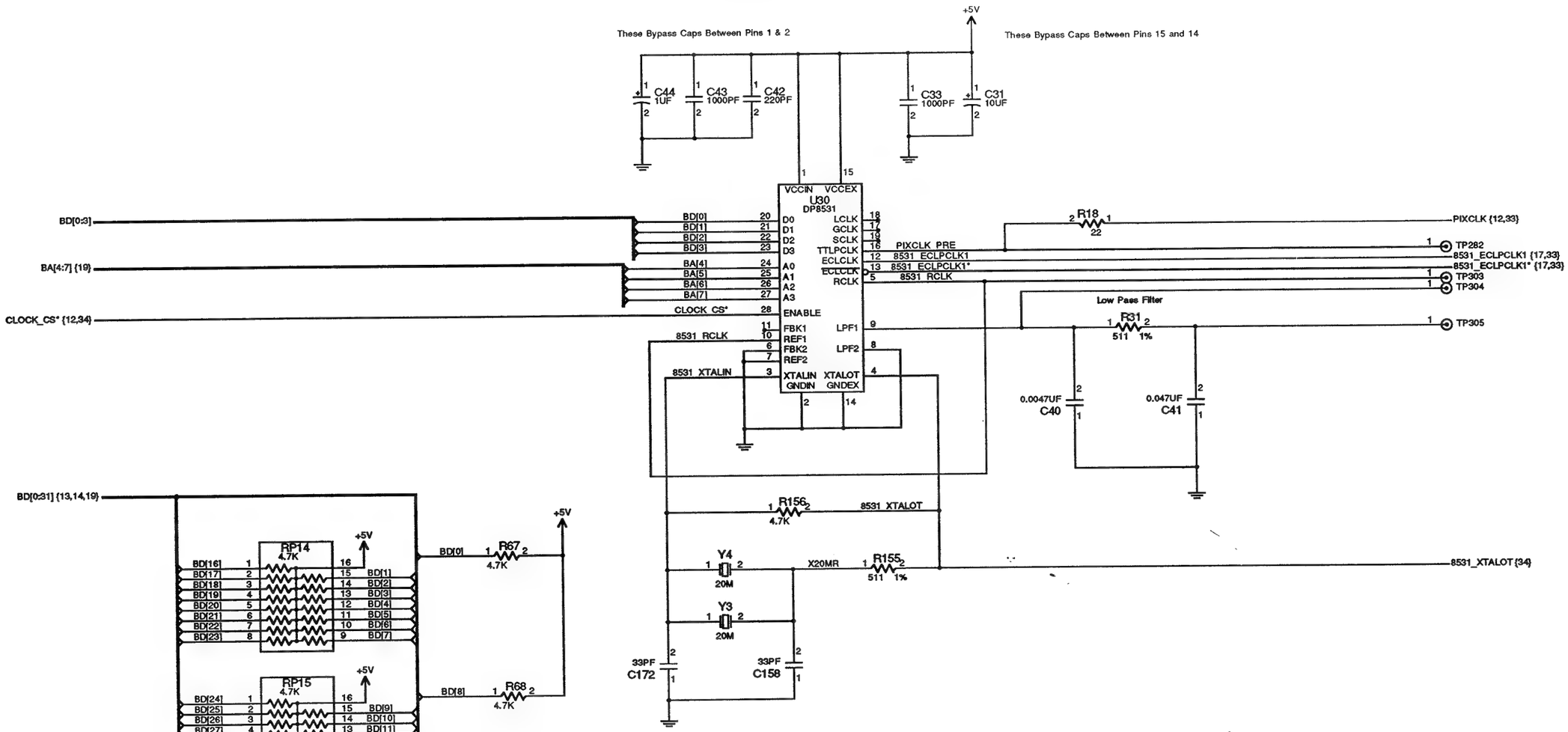

8531 Video Clock Generator
Buffered System Data Bus Pullups

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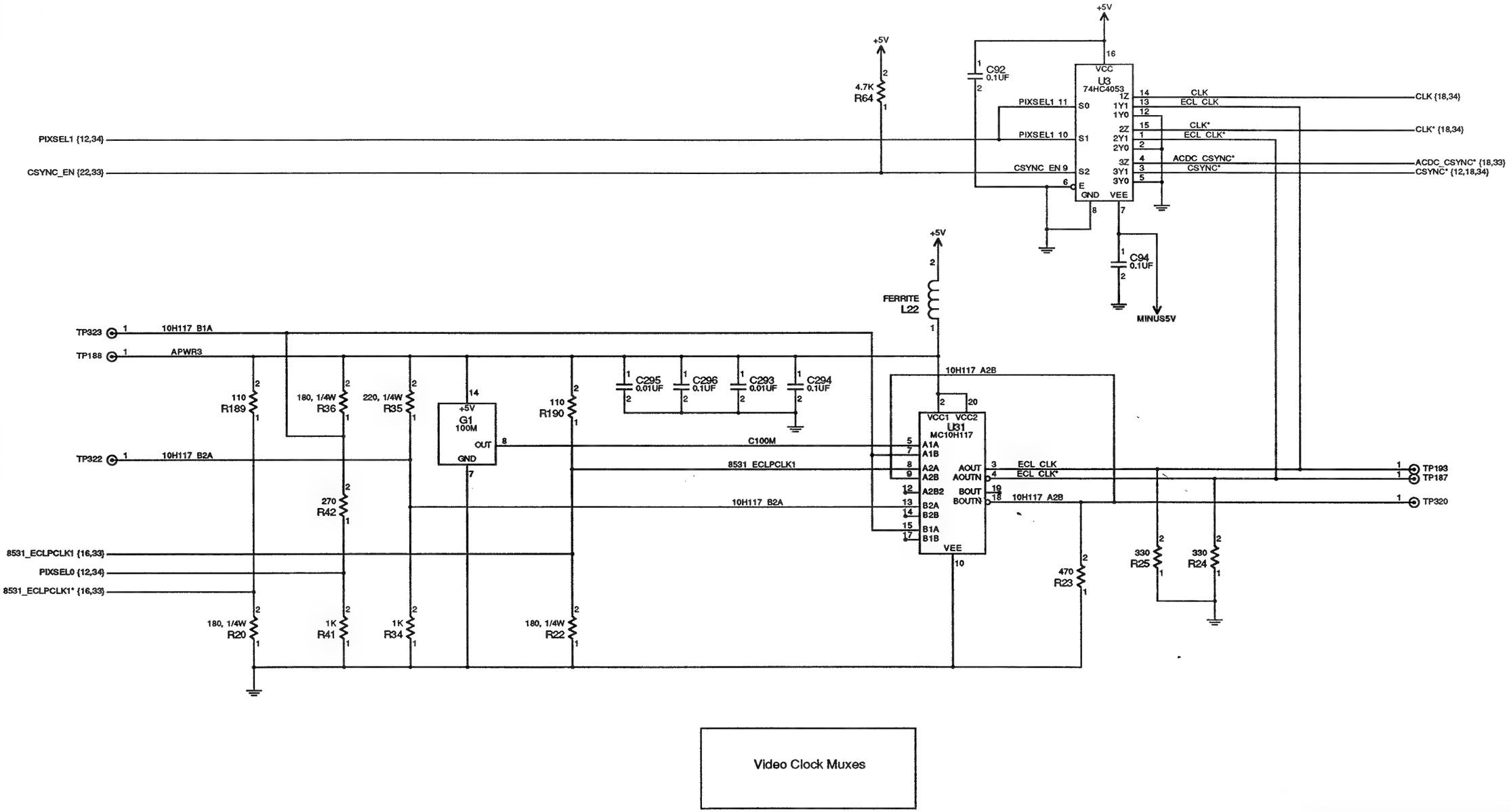

Video Clock Muxes

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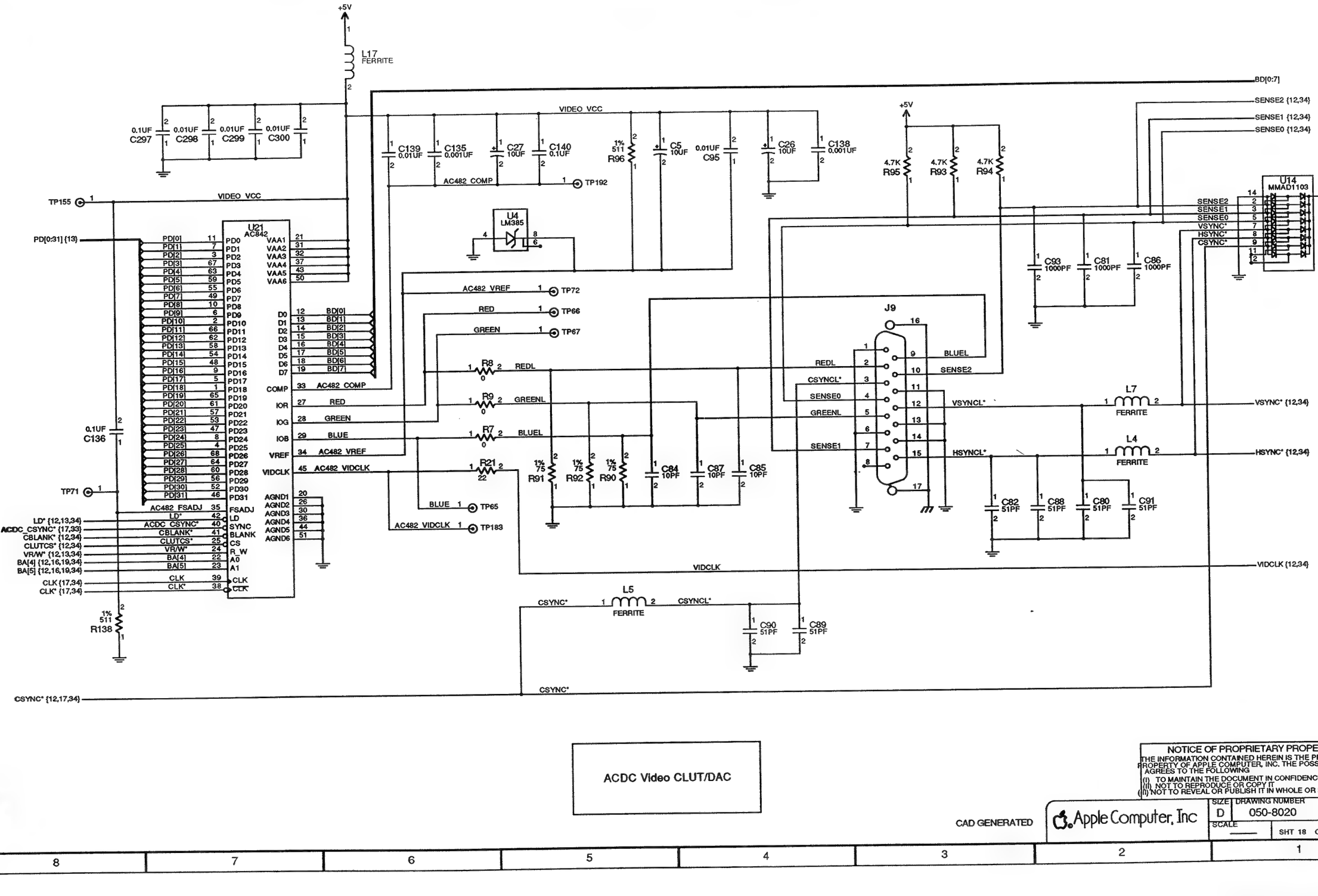

ACDC Video CLUT/DAC

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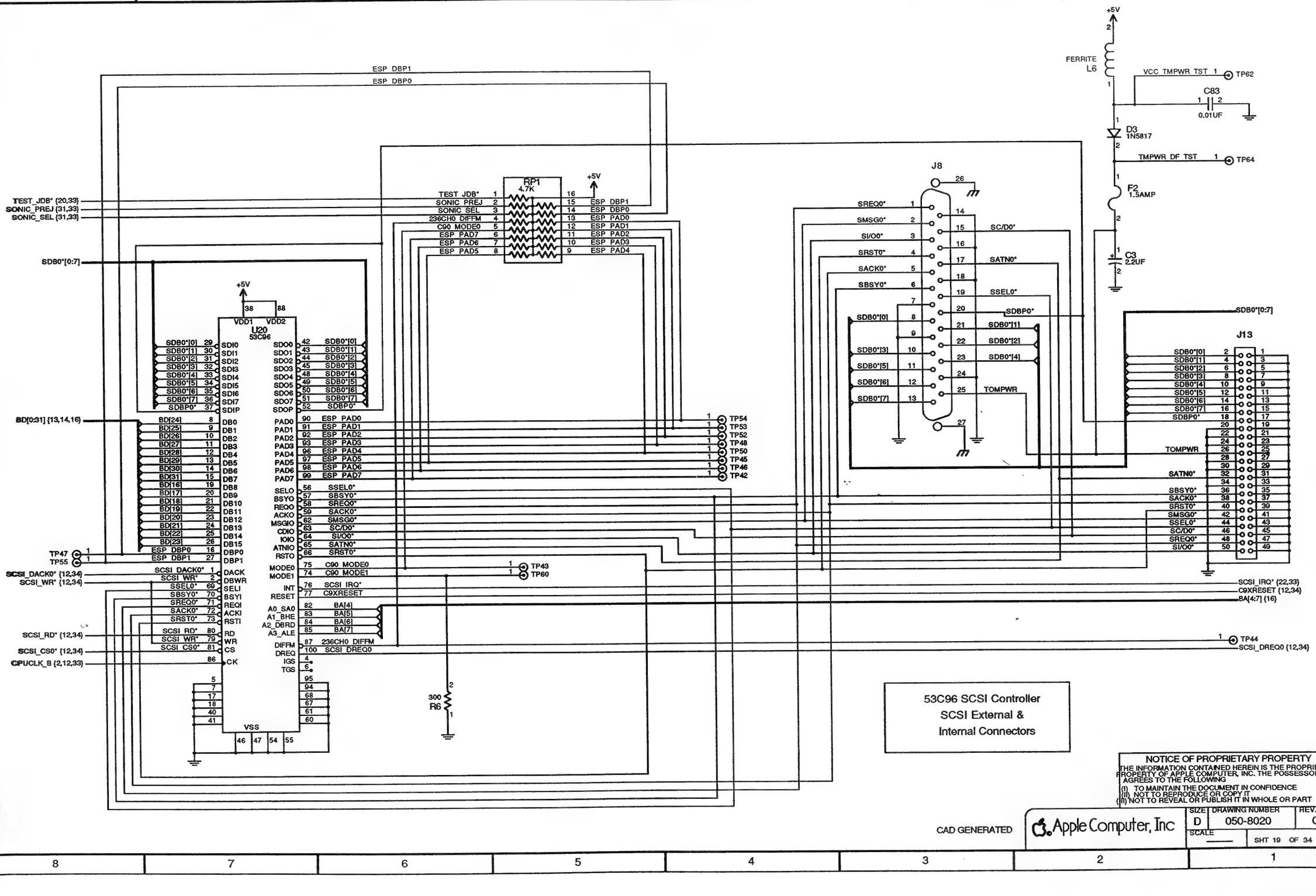
ESP DBP1
ESP DBP0
TEST_JDB* {20,33}
SONIC_PREJ {31,33}
SONIC_SEL {31,33}
SDB0*[0:7]
RP1
4.7K
+5V
TEST JDB* 1
SONIC PREJ 2
SONIC SEL 3
236CH0 DIFFM 4
C90 MODE0 5
ESP PAD7 6
ESP PAD6 7
ESP PAD5 8
16 +5V
15 ESP DBP1
14 ESP DBP0
13 ESP PAD0
12 ESP PAD1
11 ESP PAD2
10 ESP PAD3
9 ESP PAD4
U20
53C96
VDD1 VDD2
SDB0*[0] 29 SDI0
SDB0*[1] 30 SDI1
SDB0*[2] 31 SDI2
SDB0*[3] 32 SDI3
SDB0*[4] 33 SDI4
SDB0*[5] 34 SDI5
SDB0*[6] 35 SDI6
SDB0*[7] 36 SDI7
SDBP0* 37 SDIP
SDO0 42 SDB0*[0]
SDO1 43 SDB0*[1]
SDO2 44 SDB0*[2]
SDO3 45 SDB0*[3]
SDO4 48 SDB0*[4]
SDO5 49 SDB0*[5]
SDO6 50 SDB0*[6]
SDO7 51 SDB0*[7]
SDOP 52 SDBP0*
BD[0:31] {13,14,16}
BD[24] 8 DB0
BD[25] 9 DB1
BD[26] 10 DB2
BD[27] 11 DB3
BD[28] 12 DB4
BD[29] 13 DB5
BD[30] 14 DB6
BD[31] 15 DB7
BD[16] 19 DB8
BD[17] 20 DB9
BD[18] 21 DB10
BD[19] 22 DB11
BD[20] 23 DB12
BD[21] 24 DB13
BD[22] 25 DB14
BD[23] 26 DB15
ESP DBP0 16 DBP0
ESP DBP1 27 DBP1
TP47
TP55
SCSI_DACK0* {12,34}
SCSI_WR* {12,34}
SCSI_RD* {12,34}
SCSI_CS0* {12,34}
CPUCLK_B {2,12,33}
SCSI_DACK0* 1 DACK
SCSI_WR* 2 DBWR
SSEL0* 69 SELI
SBSY0* 70 BSYI
SREQ0* 71 REQI
SACK0* 72 ACKI
SRST0* 73 RSTI
SCSI_RD* 80 RD
SCSI_WR* 79 WR
SCSI_CS0* 81 CS
86 CK
PAD0 90 ESP PAD0
PAD1 91 ESP PAD1
PAD2 92 ESP PAD2
PAD3 93 ESP PAD3
PAD4 96 ESP PAD4
PAD5 97 ESP PAD5
PAD6 98 ESP PAD6
PAD7 99 ESP PAD7
SELO 56 SSEL0*
BSYO 57 SBSY0*
REQO 58 SREQ0*
ACKO 59 SACK0*
MSGIO 62 SMSG0*
CDIO 63 SC/D0*
IOIO 64 SI/O0*
ATNIO 65 SATN0*
RSTO 66 SRST0*
MODE0 75 C90 MODE0
MODE1 74 C90 MODE1
INT 76 SCSI IRQ*
RESET 77 C9XRESET
A0_SA0 82 BA[4]
A1_BHE 83 BA[5]
A2_DBRD 84 BA[6]
A3_ALE 85 BA[7]
DIFFM 87 236CH0 DIFFM
DREQ 100 SCSI DREQ0
IGS 4
TGS 6
5
7
17
18
40
41
94
68
67
61
60
VSS
46 47 54 55
TP54
TP53
TP52
TP48
TP50
TP45
TP46
TP42
TP43
TP60
300
R6
J8
SREQ0* 1
SMSG0* 2
SI/O0* 3
SRST0* 4
SACK0* 5
SBSY0* 6
7
SDB0*[0] 8
9
SDB0*[3] 10
SDB0*[5] 11
SDB0*[6] 12
SDB0*[7] 13
14
15 SC/D0*
16
17 SATN0*
18
19 SSEL0*
20 SDBP0*
21 SDB0*[1]
22 SDB0*[2]
23 SDB0*[4]
24
25 TOMPWR
26
27
+5V
FERRITE
L6
VCC TMPWR TST 1
TP62
C83
0.01UF
D3
1N5817
TMPWR DF TST 1
TP64
F2
1.5AMP
C3
2.2UF
SDB0*[0:7]
J13
SDB0*[0] 2 1
SDB0*[1] 4 3
SDB0*[2] 6 5
SDB0*[3] 8 7
SDB0*[4] 10 9
SDB0*[5] 12 11
SDB0*[6] 14 13
SDB0*[7] 16 15
SDBP0* 18 17
20 19
22 21
TOMPWR 24 23
26 25
28 27
SATN0* 30 29
32 31
34 33
SBSY0* 36 35
SACK0* 38 37
SRST0* 40 39
SMSG0* 42 41
SSEL0* 44 43
SC/D0* 46 45
SREQ0* 48 47
SI/O0* 50 49
SCSI_IRQ* {22,33}
C9XRESET {12,34}
BA[4:7] {16}
TP44
SCSI_DREQ0 {12,34}
53C96 SCSI Controller
SCSI External &
Internal Connectors
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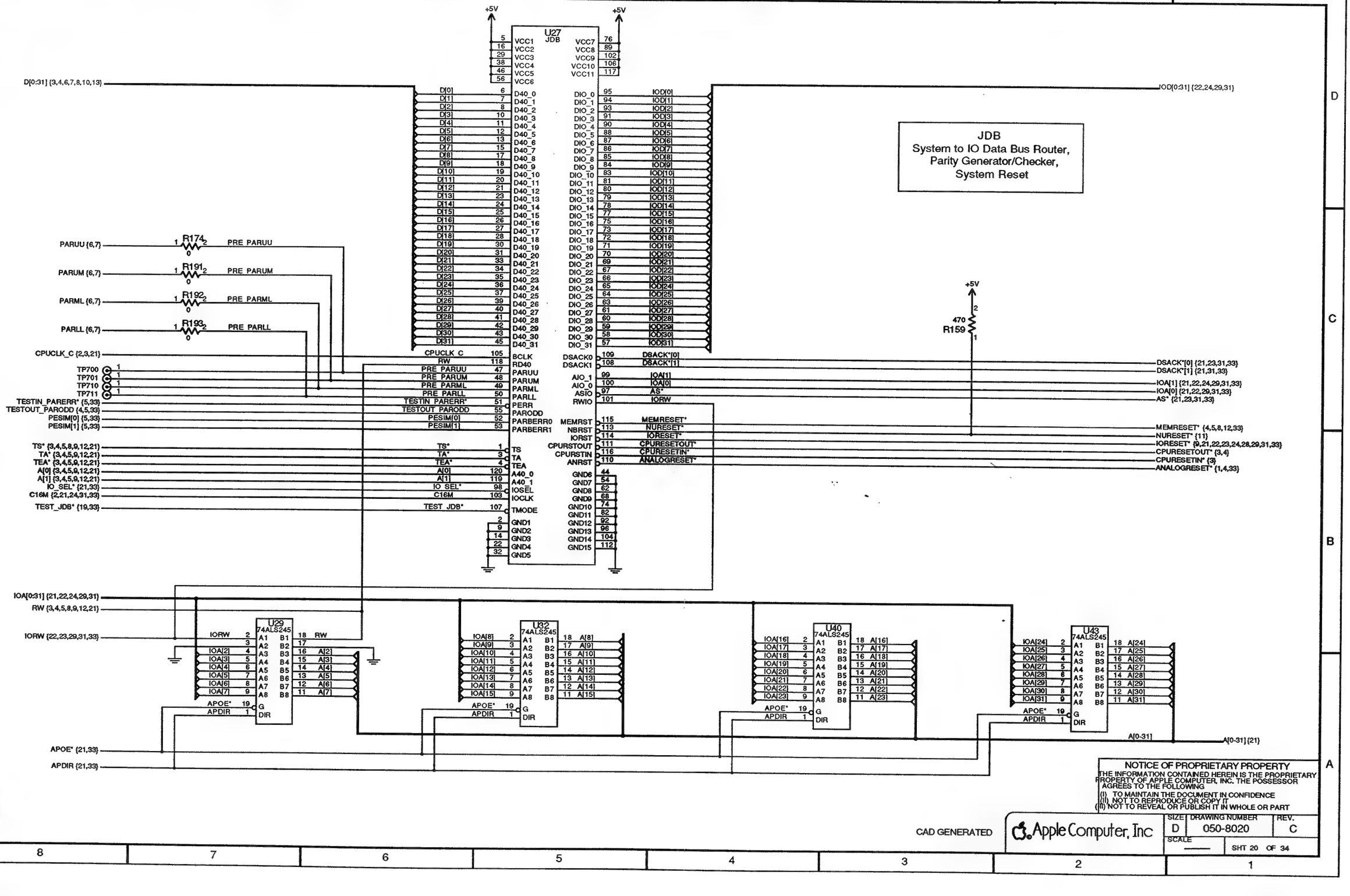
U27
JDB
+5V
VCC1
VCC2
VCC3
VCC4
VCC5
VCC6
VCC7
VCC8
VCC9
VCC10
VCC11
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
GND11
GND12
GND13
GND14
GND15
D[0:31] {3,4,6,7,8,10,13}
IOD[0:31] {22,24,29,31}
D40_0
D40_1
D40_2
D40_3
D40_4
D40_5
D40_6
D40_7
D40_8
D40_9
D40_10
D40_11
D40_12
D40_13
D40_14
D40_15
D40_16
D40_17
D40_18
D40_19
D40_20
D40_21
D40_22
D40_23
D40_24
D40_25
D40_26
D40_27
D40_28
D40_29
D40_30
D40_31
DIO_0
DIO_1
DIO_2
DIO_3
DIO_4
DIO_5
DIO_6
DIO_7
DIO_8
DIO_9
DIO_10
DIO_11
DIO_12
DIO_13
DIO_14
DIO_15
DIO_16
DIO_17
DIO_18
DIO_19
DIO_20
DIO_21
DIO_22
DIO_23
DIO_24
DIO_25
DIO_26
DIO_27
DIO_28
DIO_29
DIO_30
DIO_31
JDB
System to IO Data Bus Router,
Parity Generator/Checker,
System Reset
PARUU {6,7}
PARUM {6,7}
PARML {6,7}
PARLL {6,7}
R174
R191
R192
R193
PRE PARUU
PRE PARUM
PRE PARML
PRE PARLL
CPUCLK_C {2,3,21}
CPUCLK_C
RW
PARUU
PARUM
PARML
PARLL
TP700
TP701
TP710
TP711
TESTIN_PARERR* {5,33}
TESTOUT_PARODD {4,5,33}
PESIM[0] {5,33}
PESIM[1] {5,33}
TESTIN_PARERR*
TESTOUT_PARODD
PESIM[0]
PESIM[1]
PERR
PARODD
PARBERR0
PARBERR1
TS* {3,4,5,8,9,12,21}
TA* {3,4,5,9,12,21}
TEA* {3,4,5,9,12,21}
A[0] {3,4,5,9,12,21}
A[1] {3,4,5,9,12,21}
IO_SEL* {21,33}
C16M {2,21,24,31,33}
TEST_JDB* {19,33}
TS*
TA*
TEA*
A[0]
A[1]
IO_SEL*
C16M
TEST_JDB*
TS
TA
TEA
A40_0
A40_1
IOSEL
IOCLK
TMODE
BCLK
RD40
DSACK0
DSACK1
AIO_1
AIO_0
ASTO
RWIO
MEMRST
NBRST
IORST
CPURSTOUT
CPURSTIN
ANRST
DSACK*[0]
DSACK*[1]
IOA[1]
IOA[0]
AS*
IORW
MEMRESET*
NURESET*
IORESET*
CPURESETOUT*
CPURESETIN*
ANALOGRESET*
DSACK*[0] {21,23,31,33}
DSACK*[1] {21,31,33}
IOA[1] {21,22,24,29,31,33}
IOA[0] {21,22,29,31,33}
AS* {21,23,31,33}
MEMRESET* {4,5,8,12,33}
NURESET* {11}
IORESET* {9,21,22,23,24,28,29,31,33}
CPURESETOUT* {3,4}
CPURESETIN* {3}
ANALOGRESET* {1,4,33}
470
R159
IOA[0:31] {21,22,24,29,31}
RW {3,4,5,8,9,12,21}
IORW {22,23,29,31,33}
APOE* {21,33}
APDIR {21,33}
U29
U32
U40
U43
74ALS245
IORW
RW
APOE*
APDIR
G
DIR
A[0-31]
A[0-31] {21}
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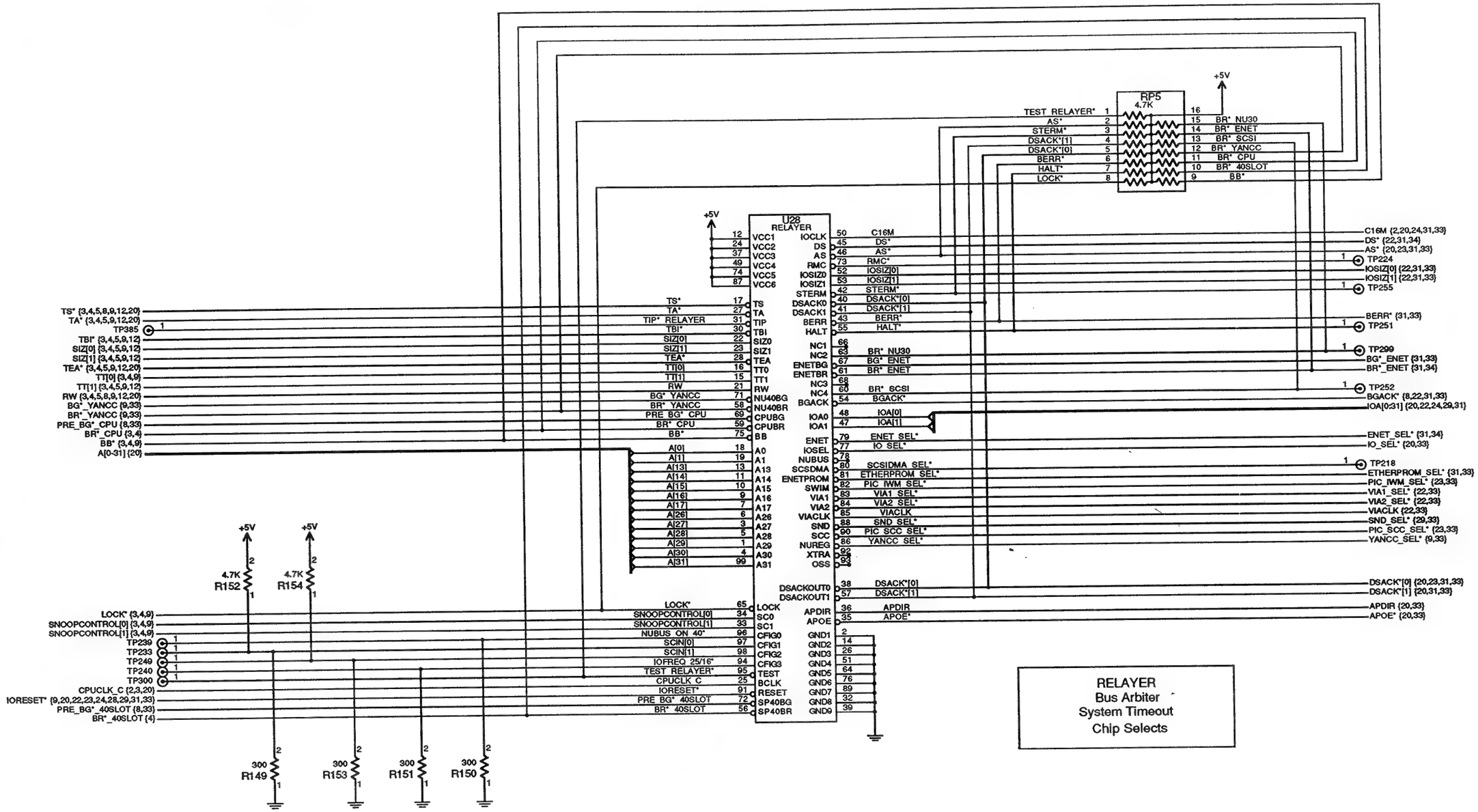

RELAYER
Bus Arbiter
System Timeout
Chip Selects

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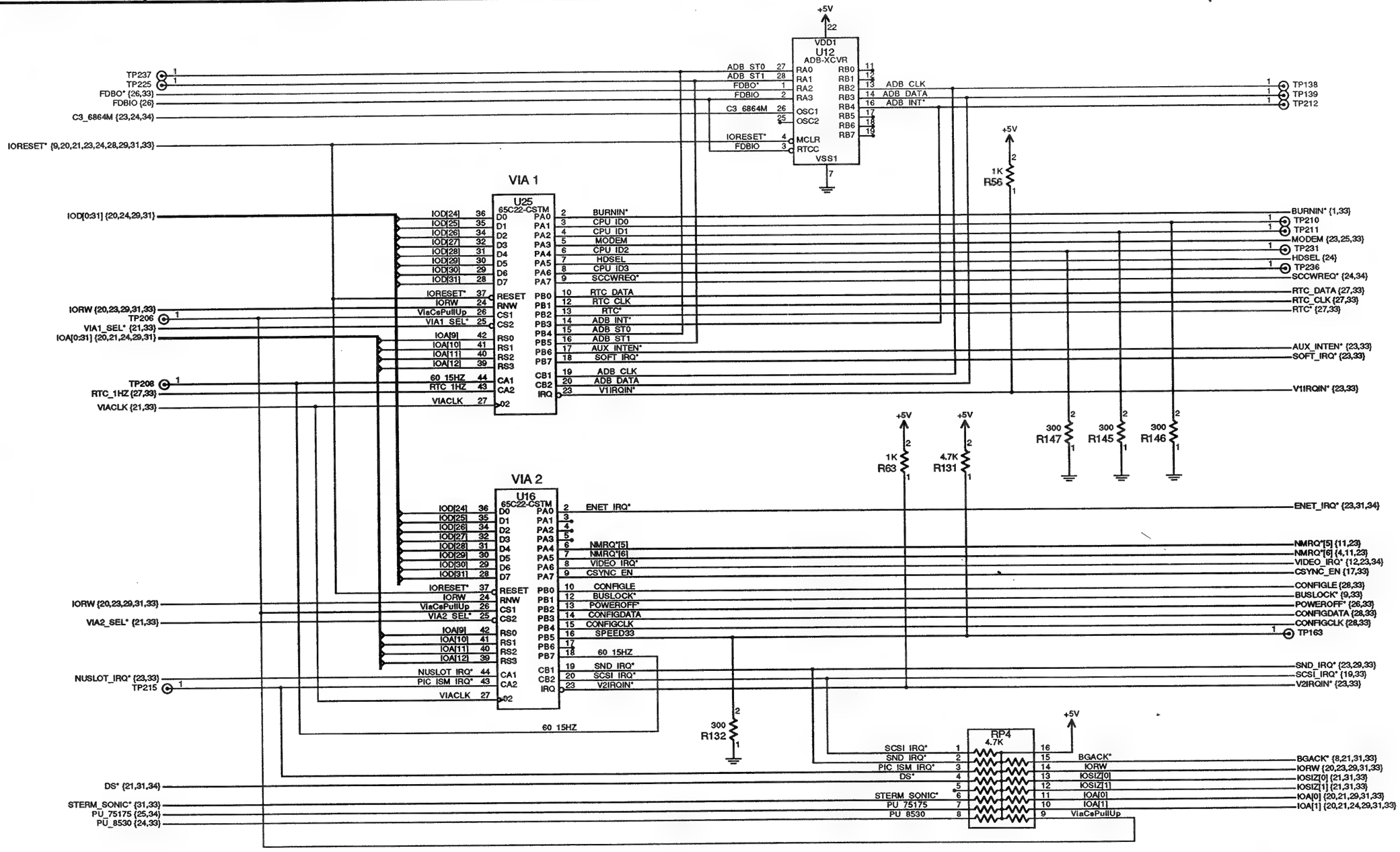

VIA 1 & 2
ADB Transceiver

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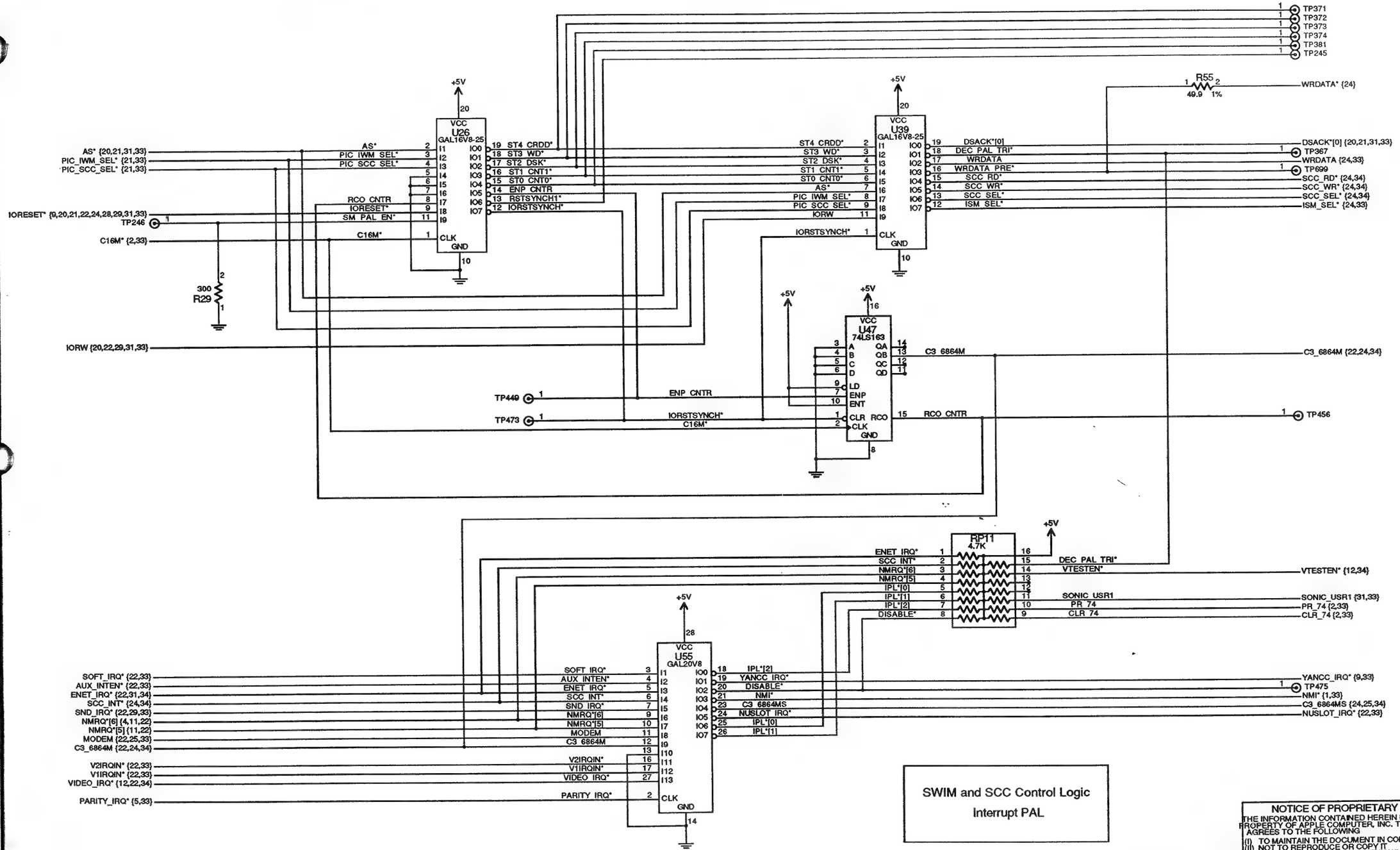
U26 GAL16V8-25
U39 GAL16V8-25
U47 74LS163
U55 GAL20V8
RP11 4.7K
R55 49.9 1%
R29 300
TP246
TP449
TP473
TP371
TP372
TP373
TP374
TP381
TP245
TP367
TP699
TP456
TP475
AS* {20,21,31,33}
PIC_IWM_SEL* {21,33}
PIC_SCC_SEL* {21,33}
IORESET* {9,20,21,22,24,28,29,31,33}
C16M* {2,33}
IORW {20,22,29,31,33}
ST4_CRDD*
ST3_WD*
ST2_DSK*
ST1_CNT1*
ST0_CNT0*
ENP_CNTR
RSTSYNCH1*
IORSTSYNCH*
RCO_CNTR
SM_PAL_EN*
C3_6864M
ENP_CNTR
IORSTSYNCH*
C16M*
RCO_CNTR
WRDATA* {24}
DSACK*[0]
WRDATA
WRDATA_PRE*
SCC_RD*
SCC_WR*
SCC_SEL*
ISM_SEL*
DSACK*[0] {20,21,31,33}
WRDATA {24,33}
SCC_RD* {24,34}
SCC_WR* {24,34}
SCC_SEL* {24,34}
ISM_SEL* {24,33}
C3_6864M {22,24,34}
RCO_CNTR {24,34}
ENET_IRQ*
SCC_INT*
NMIRQ*[6]
NMIRQ*[5]
IPL*[0]
IPL*[1]
IPL*[2]
DISABLE*
DEC_PAL_TRI*
VTESTEN*
SONIC_USR1
PR_74
CLR_74
VTESTEN* {12,34}
SONIC_USR1 {31,33}
PR_74 {2,33}
CLR_74 {2,33}
SOFT_IRQ* {22,33}
AUX_INTEN* {22,33}
ENET_IRQ* {22,31,34}
SCC_INT* {24,34}
SND_IRQ* {22,29,33}
NMIRQ*[6] {4,11,22}
NMIRQ*[5] {11,22}
MODEM {22,25,33}
C3_6864M {22,24,34}
V2IRQIN* {22,33}
V1IRQIN* {22,33}
VIDEO_IRQ* {12,22,34}
PARITY_IRQ* {5,33}
SND_IRQ*
AUX_INTEN*
SCC_INT*
NMIRQ*[6]
NMIRQ*[5]
MODEM
C3_6864M
V2IRQIN*
V1IRQIN*
VIDEO_IRQ*
PARITY_IRQ*
YANCC_IRQ*
DISABLE*
NMI*
C3_6864MS
NUSLOT_IRQ*
YANCC_IRQ* {9,33}
NMI* {1,33}
C3_6864MS {24,25,34}
NUSLOT_IRQ* {22,33}
SWIM and SCC Control Logic
Interrupt PAL
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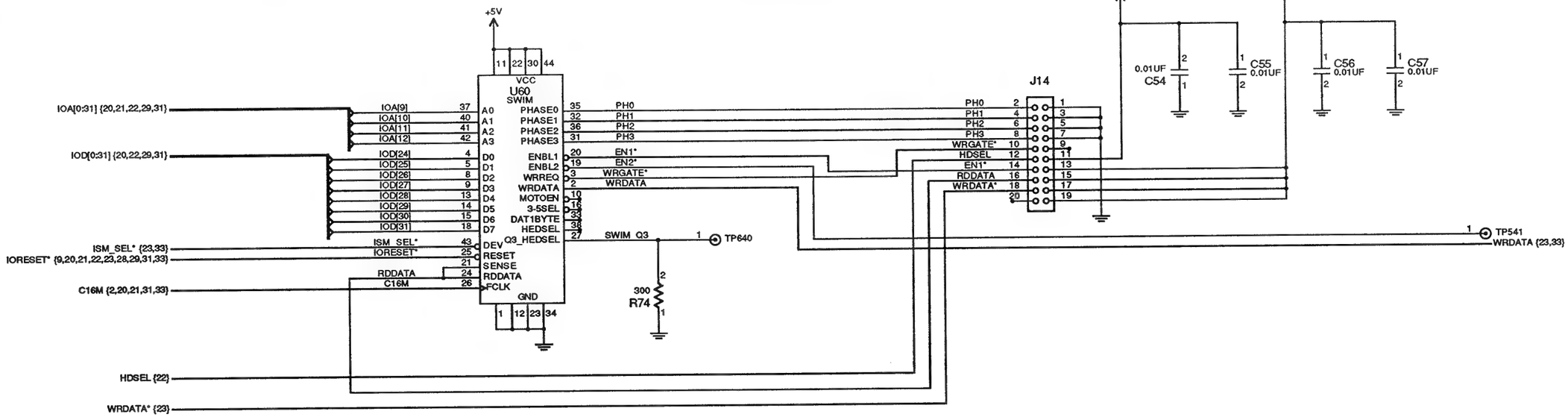

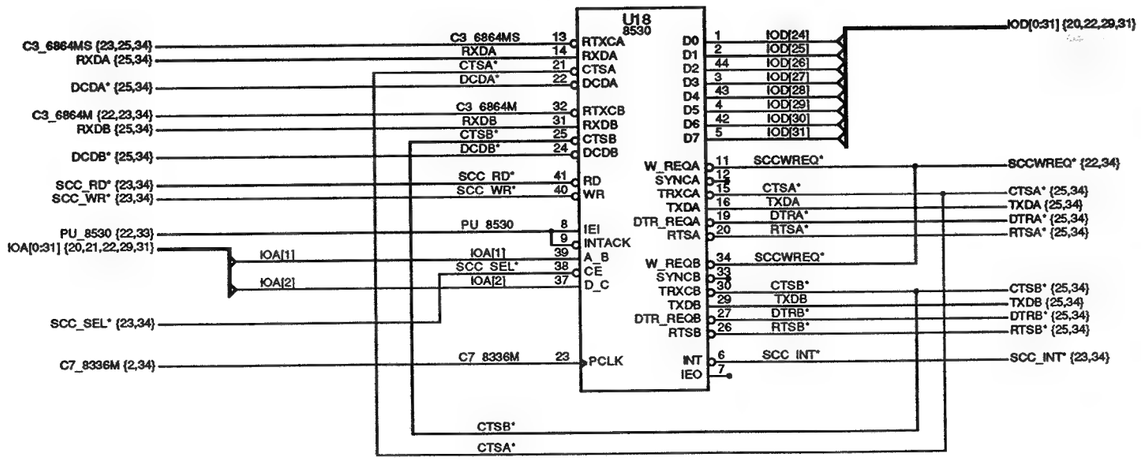

SWIM Floppy Controller
85C30

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Serial Channels – 75175s, 26LS30s

Modem
J5
J3 GPI
J3 RXD+
J3 RXDMINUS
J3 HSK1
J3 TXD+
J3 TXDMINUS
J3 HSK0
RC1
25-150PF
J3 TXDMINUS
J3 TXD+
J3 GPI
J3 RXD+
J3 RXDMINUS
J3 HSK1
J3 HSK0
TXDAMINUS
TXDA+
GPIA
RXDA+
RXDAMINUS
HSKIA
HSKOA
TP36
TP31
TP25
TP23
TP22
TP20
TP119
+5V
L13
FERRITE
C18
1.5pF
C30
1.5pF
VCCLS301 TP
TP129
VCC
U11
26LS30
TXDA {24,34}
RTSA* {24,34}
DTRA* {24,34}
TP132
TP21
TXDA
RTSA*
DTRA*
SRA TST1
SRB TST1
INA
INB
INC
IND
SRA
SRB
SRC
SRD
GND
OUTA
OUTB
OUTC
OUTD
MODE
VEE
TXDA+
TXDAMINUS
HSKOA
TP137
L12
FERRITE
0.01UF
C117
MINUS5V
+5V
L11
FERRITE
VCCLS302 TP
TP136
VCC
U13
26LS30
TXDB {24,34}
RTSB* {24,34}
DTRB* {24,34}
TP154
TP39
TXDB
RTSB*
DTRB*
SRA TST2
SRB TST2
TXDB+
TXDBMINUS
HSKOB
1.5pF
C29
1.5pF
C24
VEELS302 TP
TP178
0.01UF
C25
L14
FERRITE
MINUS5V
+5V
R165
100K
+5V
R168
100K
+5V
16
VCC1
U1
75175
RXDA+
RXDAMINUS
HSKIA
PD13
GPIA
PU 75175
MODEM
1A
1B
2A
2B
3A
3B
4A
4B
EN1
EN2
GND1
1Y
2Y
3Y
4Y
RXDA
CTSA*
C3_6864MS
RXDA {24,34}
CTSA* {24,34}
C3_6864MS {23,24,34}
PU_75175 {22,34}
+5V
16
VCC1
U2
75175
RXDB+
RXDBMINUS
HSKIB
GPIB
GPIA
PU 75175
RXDB
CTSB*
DCDB*
DCDA*
RXDB {24,34}
CTSB* {24,34}
DCDB* {24,34}
DCDA* {24,34}
R13
300
J6
Printer
J4 GPI
J4 RXD+
J4 RXDMINUS
J4 HSK1
J4 TXD+
J4 TXDMINUS
J4 HSK0
RC2
25-150PF
J4 TXDMINUS
J4 TXD+
J4 GPI
J4 RXD+
J4 RXDMINUS
J4 HSK1
J4 HSK0
TXDBMINUS
TXDB+
GPIB
RXDB+
RXDBMINUS
HSKIB
HSKOB
TP38
TP41
TP27
TP33
TP32
TP37
TP40
MODEM {22,23,33}
TP18

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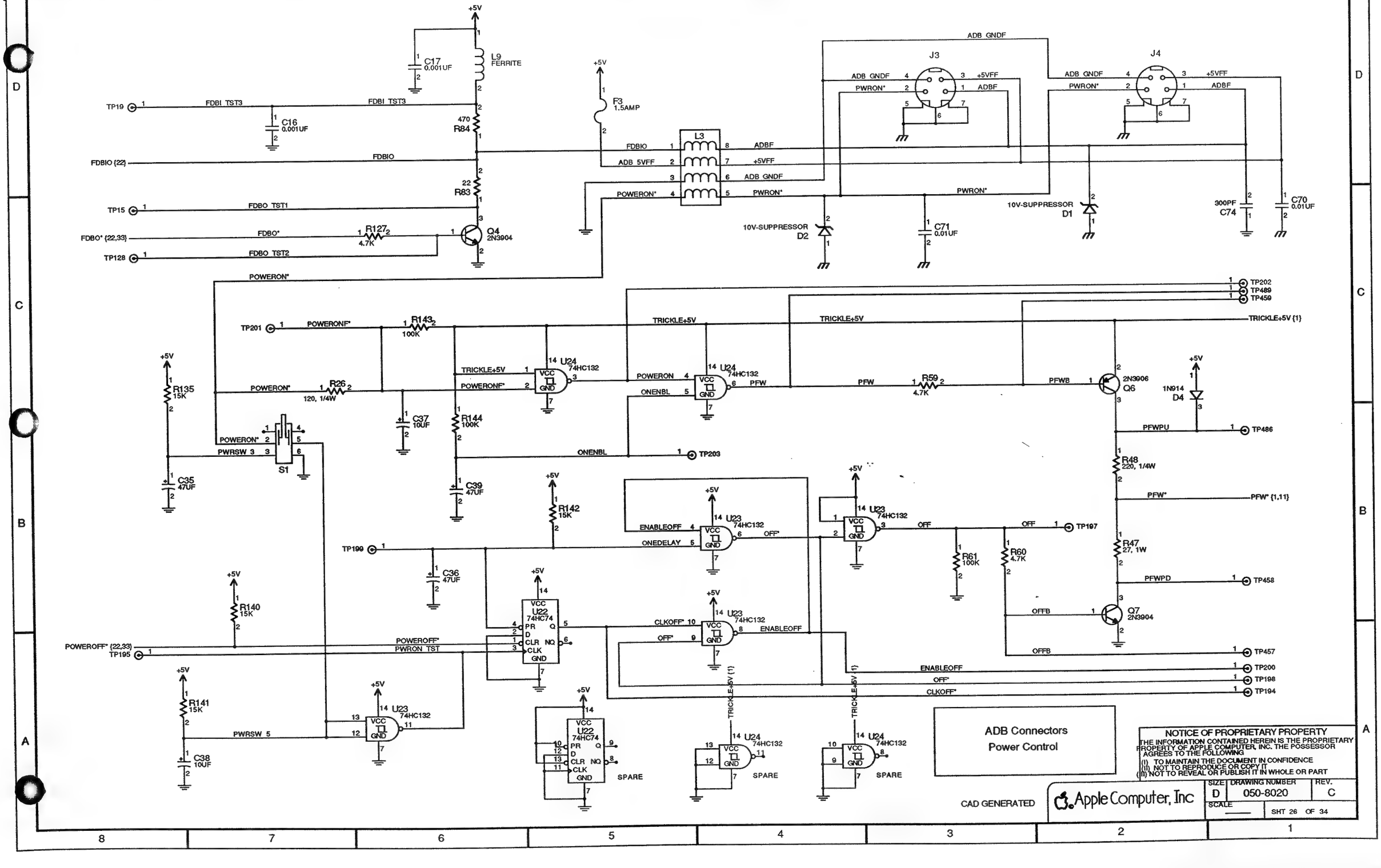

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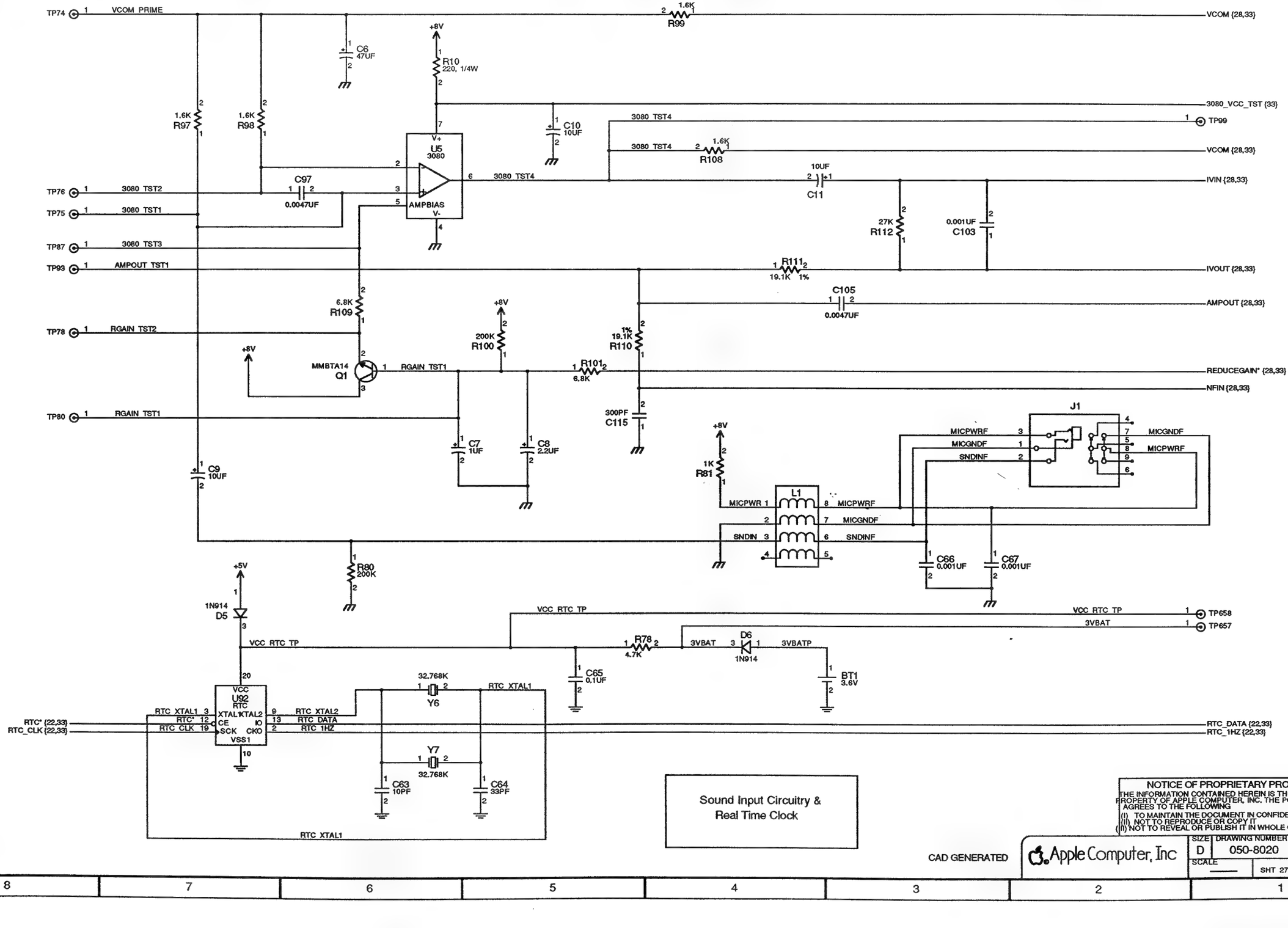
TP74 1 VCOM PRIME
R99 1.6K
VCOM {28,33}
C6 47UF
+8V
R10 220, 1/4W
3080_VCC_TST {33}
R97 1.6K
R98 1.6K
C10 10UF
3080 TST4
TP99
U5 3080
V+
AMPBIAS
V-
R108 1.6K
VCOM {28,33}
TP76 1 3080 TST2
C97 0.0047UF
C11 10UF
IVIN {28,33}
TP75 1 3080 TST1
R112 27K
C103 0.001UF
TP87 1 3080 TST3
TP93 1 AMPOUT TST1
R111 19.1K 1%
IVOUT {28,33}
C105 0.0047UF
AMPOUT {28,33}
R109 6.8K
TP78 1 RGAIN TST2
200K R100
R110 19.1K 1%
MMBTA14 Q1
RGAIN TST1
R101 6.8K
REDUCEGAIN* {28,33}
NFIN {28,33}
300PF C115
TP80 1 RGAIN TST1
C7 1UF
C8 2.2UF
C9 10UF
J1
MICPWRF
MICGNDF
SNDINF
1K R81
L1
MICPWR 1
SNDIN 3
R80 200K
C66 0.001UF
C67 0.001UF
+5V
1N914 D5
VCC RTC TP
TP658
3VBAT
TP657
R78 4.7K
D6 1N914
3VBATP
BT1 3.6V
C65 0.1UF
32.768K Y6
U92 RTC
VCC
XTAL1
XTAL2
CE
SCK
CKO
IO
VSS1
RTC_XTAL1
RTC_XTAL2
RTC_DATA
RTC_1HZ
RTC* {22,33}
RTC_CLK {22,33}
RTC_DATA {22,33}
RTC_1HZ {22,33}
Y7 32.768K
C63 10PF
C64 33PF
Sound Input Circuitry & Real Time Clock
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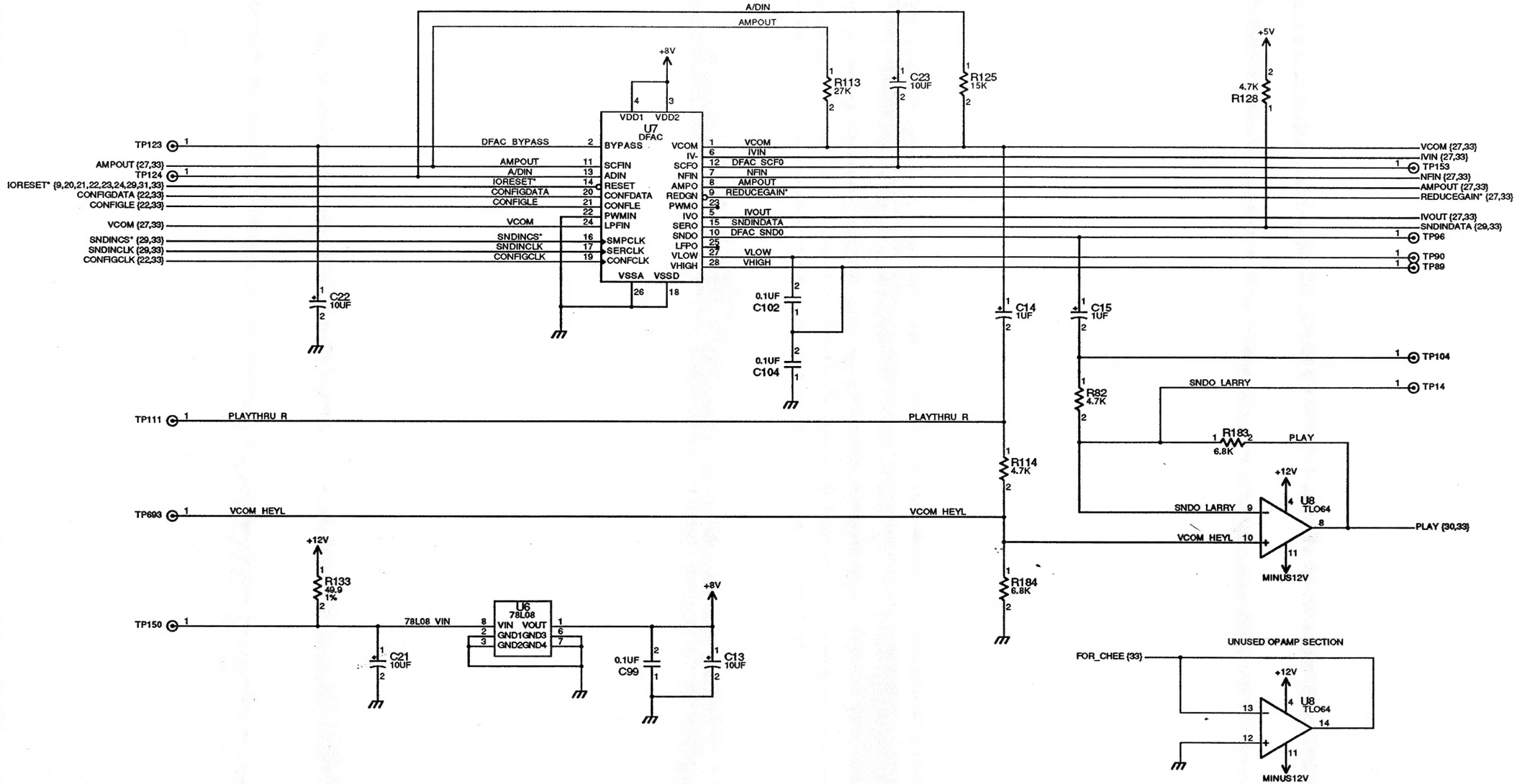

DFAC Sound In

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L10
FERRITE
LINKS CHASSIS TO GND

+5V
L15
FERRITE
TP156
VCC_BATMAN
C120 0.01UF
C28 47UF
C119 0.001UF

U15
E_APPLE SOUND
VDD
GND
IOA[0:31] {20,21,22,24,31}
IOA[0] IOA[1] IOA[2] IOA[3] IOA[4] IOA[5] IOA[6] IOA[7] IOA[8] IOA[9] IOA[10] IOA[11]
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11
IORESET* {9,20,21,22,23,24,28,31,33}
SND_SEL* {21,33}
IORW {20,22,23,31,33}
SNDINDATA {28,33}
IORESET* SND_SEL* IORW SNDINDATA
POC CS R_W SERIN DOS XTALIN
PWMA_SEROUT PWMB_SROTCL SRCLK SRINCLK SERINCS INT XTALOUT
SV0 SV1 SV2
D0 D1 D2 D3 D4 D5 D6 D7
SV0 PRE
SV1 PRE
SV2 PRE
IOD[24] IOD[25] IOD[26] IOD[27] IOD[28] IOD[29] IOD[30] IOD[31]
PRESEROUT
PRE_SEROUTCLK
PRE_SERCLK
SNDINCLK
SNDINCS*
SND_IRQ*
XTALOUT

XTALIN
Y1 22.5792M
Y2 22.5792M
R148 1M
XTALOUT

33PF C147
33PF C148
TP221 XTLO_TP
33PF C146
33PF C145
TP217 XTLI_TP

R188 49.9 1%
R130 49.9 1%
R129 49.9 1%

SV0_PRE 220, 1/4W R185
SV1_PRE 220, 1/4W R186
SV2_PRE 220, 1/4W R187
SV0 {30,33}
SV1 {30,33}
SV2 {30,33}
SV0_PRE TP695
SV1_PRE TP696
SV2_PRE TP697
IOD[0:31] {20,22,24,31}

56PF C303
56PF C302
56PF C301

TP115
TP135
SNDINCLK {28,33}
SNDINCS* {28,33}
SND_IRQ* {22,23,33}
TP694

SPORTY_AINR
SPORTY_AINR {30,33}
C108 0.01UF
1% 866 R116
+12V
U8 TLO64
TDA1543_AOR
SPORTY_OFFADJ
0.01UF C107
MINUS12V
C109 0.01UF
TDA1543_AOL
SPORTY_AINL {30,33}
1% 866 R123
C111 0.01UF
TP130
TP121
SPORTY_OFFADJ {30,33}
3.9K R124

Sporty_5VRef {30,33}
TP134 SEROUTCLK
TP133 SRCLK
TP131 SerOut
U10 TDA1543
VDD RCK WS DATAGND
Sporty_5VRef SEROUTCLK SRCLK SerOut
AOL AOR VREF
TDA1543_AOL TDA1543_AOR SPORTY_OFFADJ

56PF C113
56PF C114
56PF C106

Batman Sound

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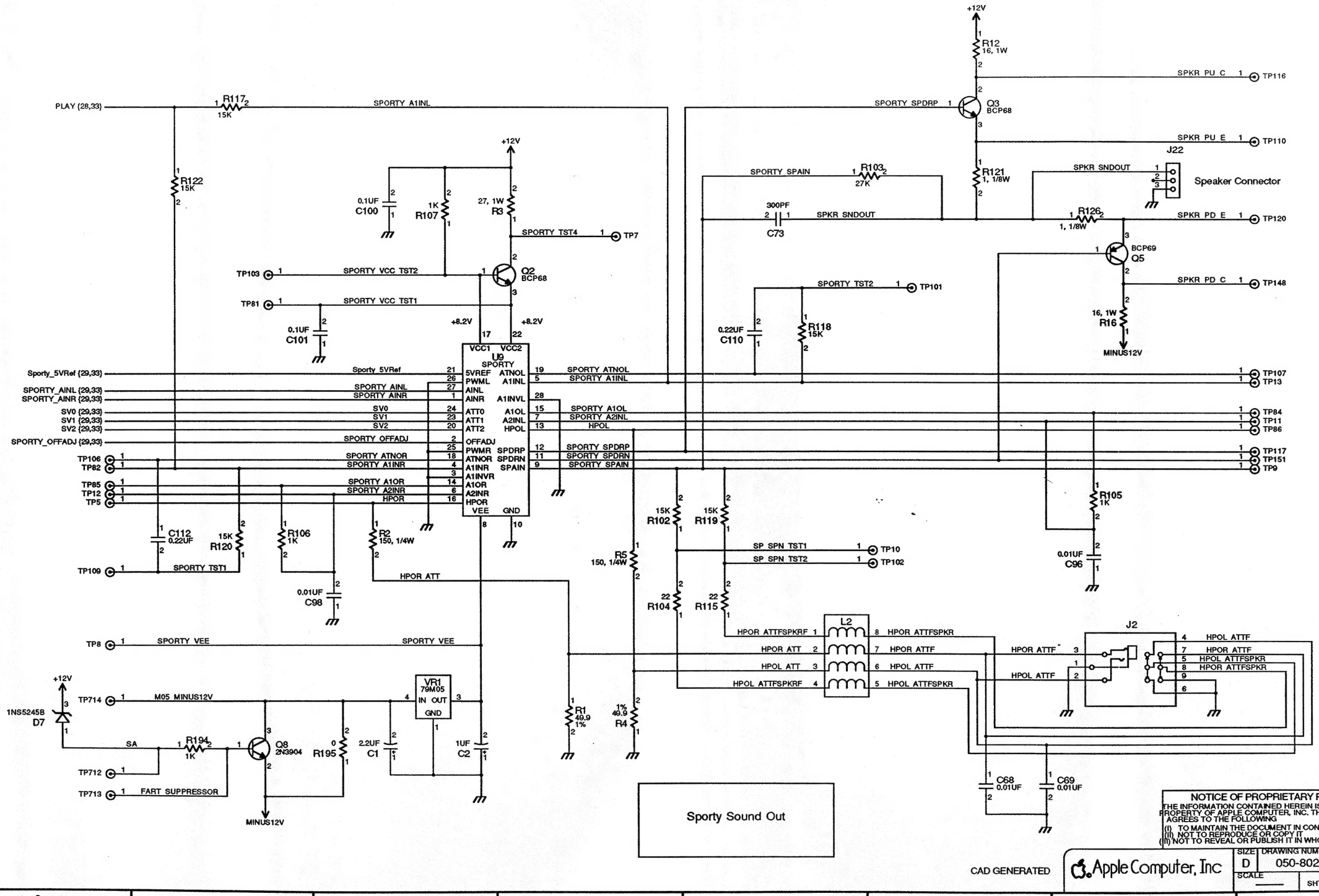
PLAY {28,33}
R117 15K
SPORTY A1INL
R122 15K
+12V
0.1UF C100
1K R107
27, 1W R3
SPORTY TST4
TP7
TP103
SPORTY VCC TST2
Q2 BCP68
TP81
SPORTY VCC TST1
0.1UF C101
+8.2V
+8.2V
VCC1 VCC2
U9 SPORTY
Sporty_5VRef {29,33}
Sporty_5VRef
5VREF ATNOL
PWML A1INL
SPORTY_AINL {29,33}
SPORTY_AINR {29,33}
SPORTY AINL
SPORTY AINR
AINL
AINR A1INVL
SV0 {29,33}
SV1 {29,33}
SV2 {29,33}
SV0
SV1
SV2
ATT0 A1OL
ATT1 A2INL
ATT2 HPOL
SPORTY_OFFADJ {29,33}
SPORTY OFFADJ
OFFADJ
PWMR SPDRP
ATNOR SPDRN
A1INR SPAIN
A1INVR
A1OR
A2INR
HPOR
VEE GND
SPORTY ATNOR
SPORTY A1INR
SPORTY A1OR
SPORTY A2INR
HPOR
SPORTY ATNOL
SPORTY A1INL
SPORTY A1OL
SPORTY A2INL
HPOL
SPORTY SPDRP
SPORTY SPDRN
SPORTY SPAIN
TP106
TP82
TP85
TP12
TP5
C112 0.22UF
15K R120
R106 1K
R2 150, 1/4W
TP109
SPORTY TST1
0.01UF C98
HPOR ATT
TP8
SPORTY VEE
SPORTY VEE
+12V
1NS5245B D7
TP714
M05 MINUS12V
VR1 79M05
IN OUT
GND
SA
R194 1K
Q8 2N3904
R195 0
2.2UF C1
1UF C2
TP712
TP713
FART SUPPRESSOR
MINUS12V
R1 49.9 1%
1% 49.9 R4
R5 150, 1/4W
15K R102
15K R119
22 R104
22 R115
SP SPN TST1
SP SPN TST2
TP10
TP102
L2
HPOR ATTFSPKRF
HPOR ATT
HPOL ATT
HPOL ATTFSPKRF
HPOR ATTFSPKR
HPOR ATTF
HPOL ATTF
HPOL ATTFSPKR
J2
C68 0.01UF
C69 0.01UF
+12V
R12 16, 1W
SPKR PU C
TP116
SPORTY SPDRP
Q3 BCP68
SPKR PU E
TP110
J22
Speaker Connector
SPORTY SPAIN
R103 27K
R121 1, 1/8W
SPKR SNDOUT
300PF C73
SPKR SNDOUT
R126 1, 1/8W
SPKR PD E
TP120
BCP69 Q5
SPKR PD C
TP148
SPORTY TST2
TP101
0.22UF C110
R118 15K
16, 1W R16
MINUS12V
TP107
TP13
TP84
TP11
TP86
TP117
TP151
TP9
R105 1K
0.01UF C96
Sporty Sound Out
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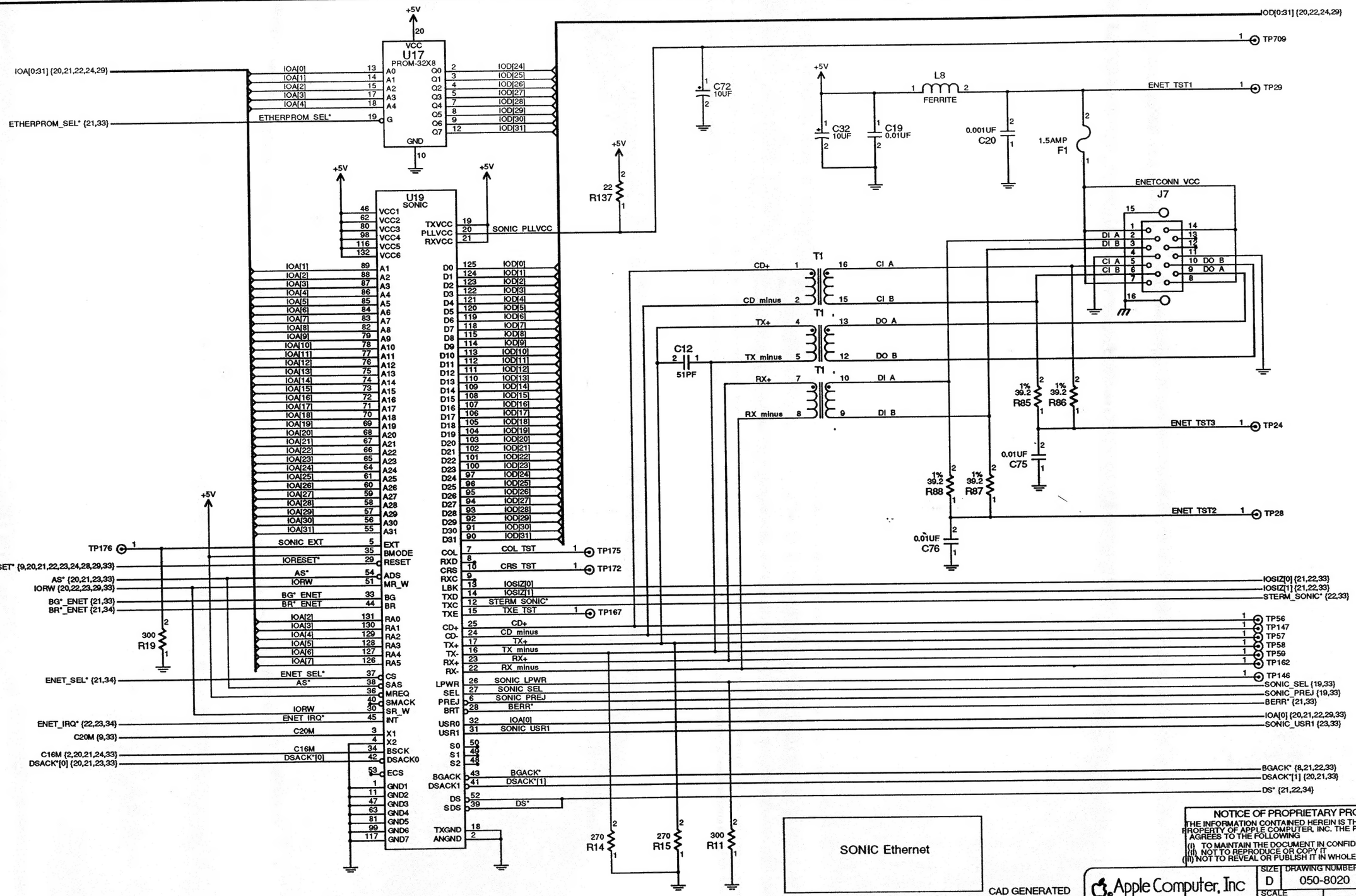
U17
PROM-32X8
U19
SONIC
ETHERPROM_SEL*
SONIC PLLVCC
SONIC EXT
IORESET*
AS*
IORW
BG* ENET
BR* ENET
ENET_SEL*
ENET_IRQ*
C20M
C16M
DSACK*[0]
R19
300
C72
10UF
L8
FERRITE
C32
10UF
C19
0.01UF
C20
0.001UF
F1
1.5AMP
ENETCONN VCC
J7
ENET TST1
ENET TST3
ENET TST2
R85
R86
R87
R88
C75
C76
T1
C12
51PF
R137
22
R14
270
R15
270
R11
300
TP709
TP29
TP24
TP28
TP176
TP175
TP172
TP167
TP56
TP147
TP57
TP58
TP59
TP162
TP146
IOD[0:31] {20,22,24,29}
IOA[0:31] {20,21,22,24,29}
ETHERPROM_SEL* {21,33}
IOSIZ[0] {21,22,33}
IOSIZ[1] {21,22,33}
STERM_SONIC* {22,33}
SONIC_SEL {19,33}
SONIC_PREJ {19,33}
BERR* {21,33}
IOA[0] {20,21,22,29,33}
SONIC_USR1 {23,33}
BGACK* {8,21,22,33}
DSACK*[1] {20,21,33}
DS* {21,22,34}
IORESET* {9,20,21,22,23,24,28,29,33}
AS* {20,21,23,33}
IORW {20,22,23,29,33}
BG* ENET {21,33}
BR* ENET {21,34}
ENET_SEL* {21,34}
ENET_IRQ* {22,23,34}
C20M {9,33}
C16M {2,20,21,24,33}
DSACK*[0] {20,21,23,33}
SONIC Ethernet
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